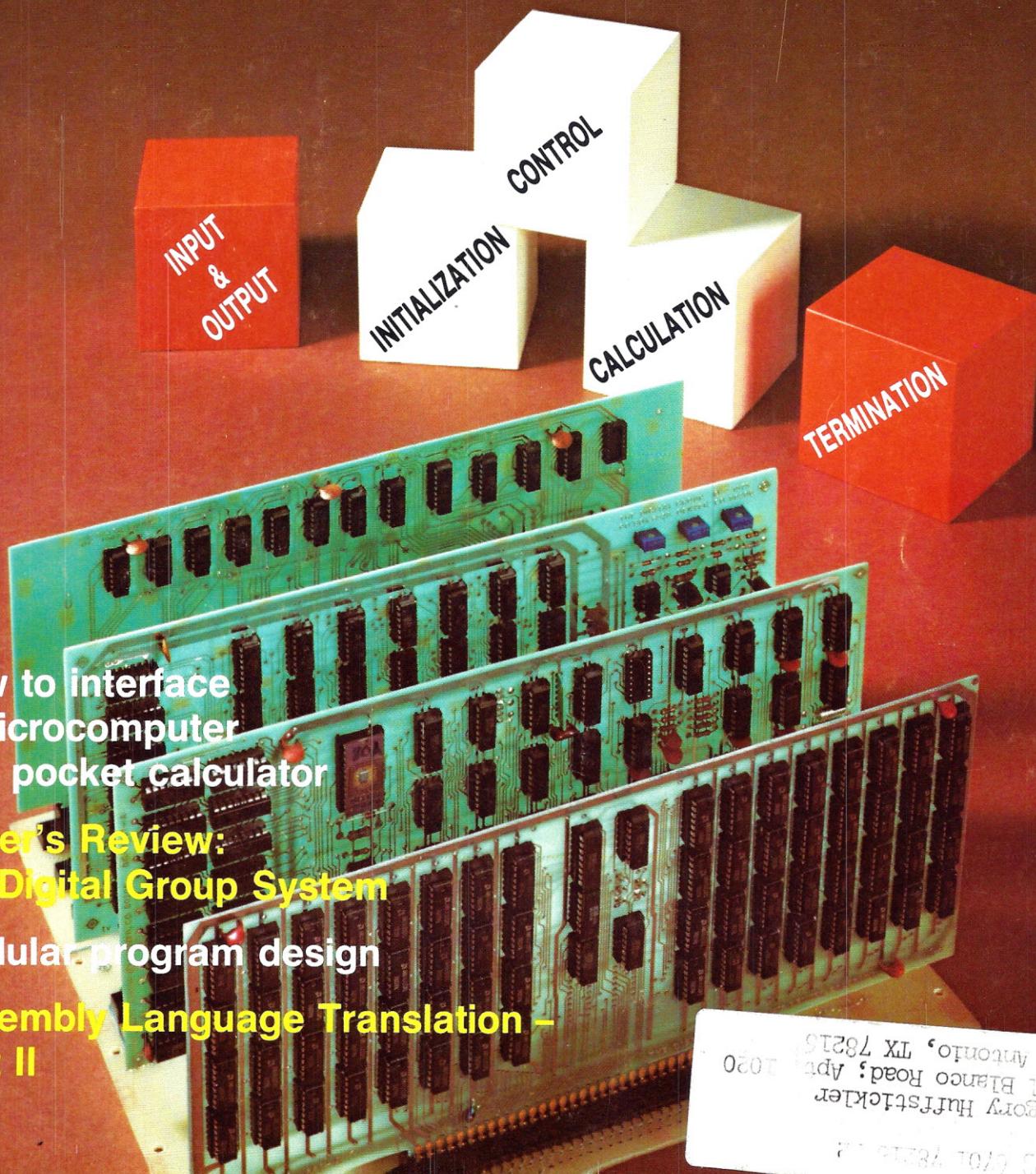


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Modular program design

**Assembly Language Translation –
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| | FOR |

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| | |
|------------|-------------|
| END | STOP |
| GOTO* | ON...GOTO* |
| | ON...GOSUB* |
| | PATCH* |
| IF...THEN* | RETURN |
| INPUT | † DES |
| PRINT* | † PEEK |
| NEXT | † POKE |

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| | | |
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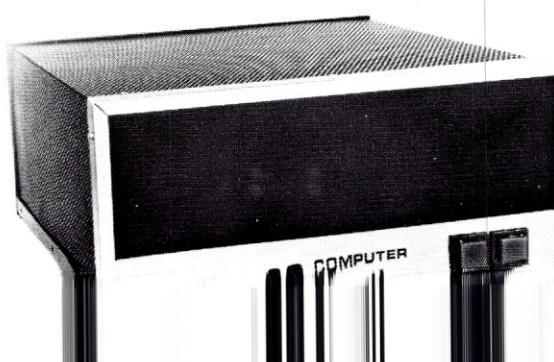
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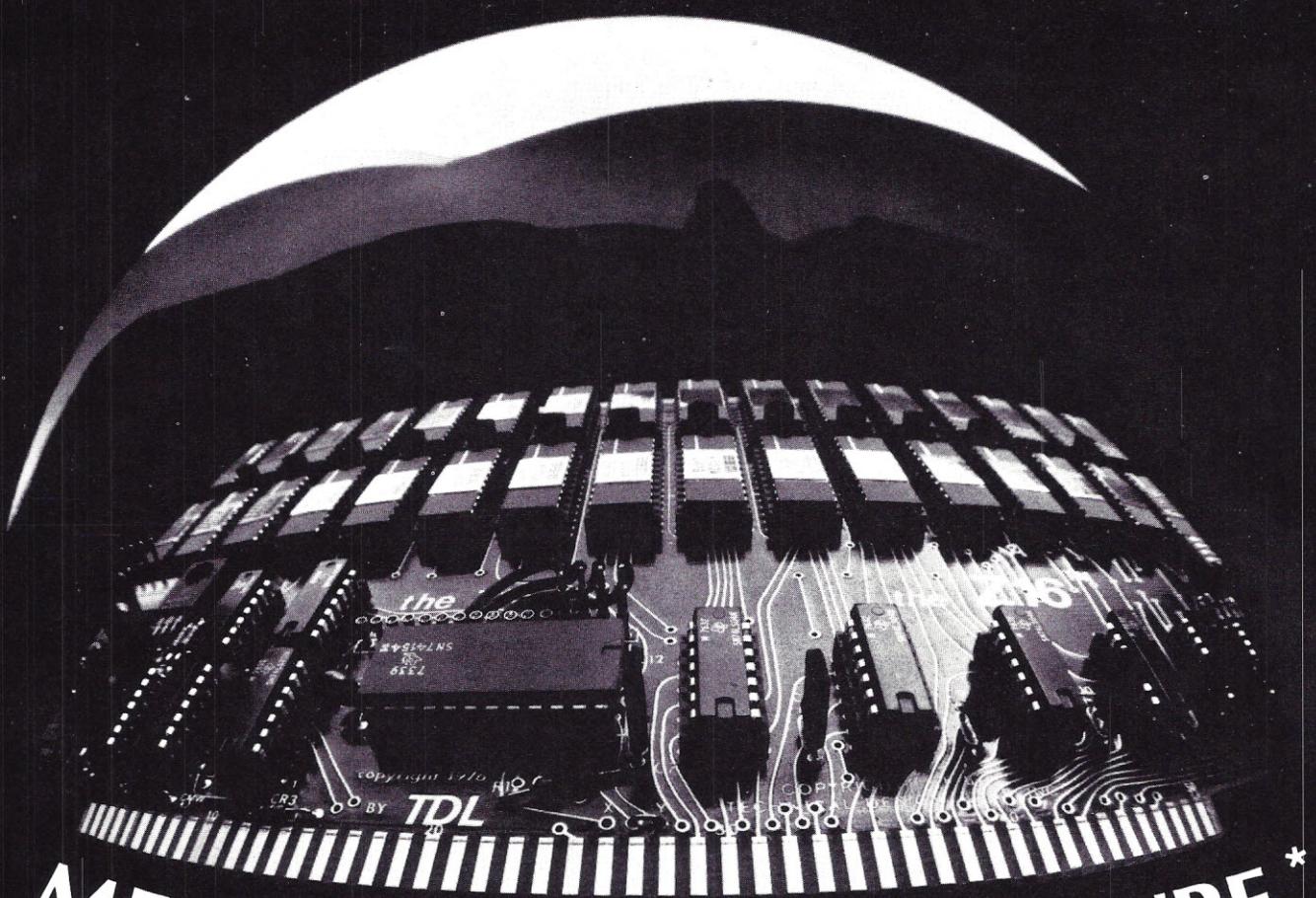
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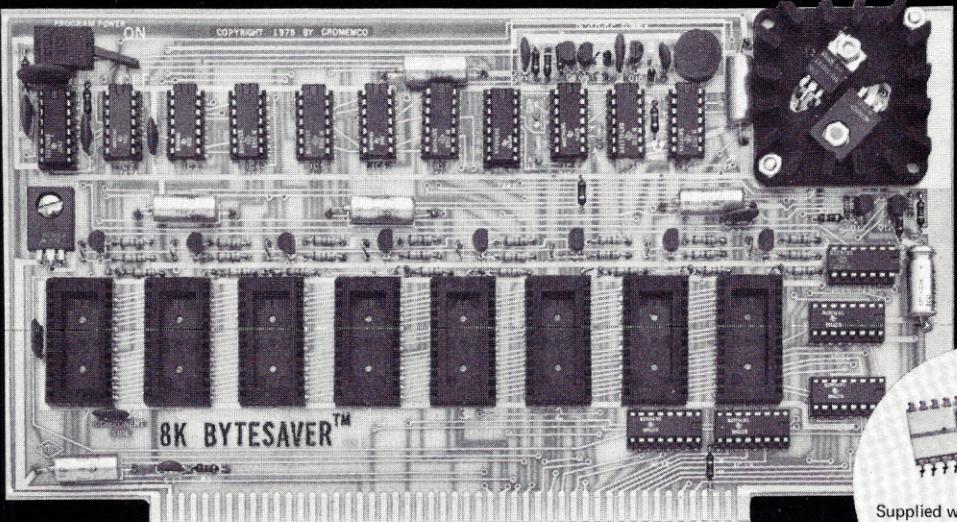
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Our source listings contain comments throughout, label table, hex code dump complete instructions, and sample output. External references (to MIKBUG routines) are easily modified. When ordering add \$1 postage and handling under \$10, 5% for first class mail, 4% sales tax (Ind. residents). Personal checks will clear bank. Many other programs, for information send SASE.

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Modular Program Design, by Steve A. Hughes, Joe Celko, and Elizabeth Hughes. Does program design appear to be an inscrutable black art? Are you bedeviled by mysterious program failures? If so, exorcise those programming poltergeists and dispel your software superstitions with this scientific approach to program design. It's as easy as the game of tic-tac-toe which is used to illustrate this program design technique 8

Interfacing a Microcomputer to a Pocket Calculator, by Michael Wimble. Add powerful mathematical functions to your computer's capabilities without tedious software development or expensive components. A general approach to calculator interfacing, complete with specific hardware techniques, serves as a valuable guide for the implementation of mathematical functions under computer control with minimum cost 21

Buyer's Report: The Digital Group System, by Steven R. Woodall. A critical review of the Z-80 version of the Digital Group System is presented. User convenience and operating software, often overlooked in published reviews, is considered here and is critiqued as a valuable system resource. Read this article to see if a Digital Group computer lies in your future. 35

Introduction to Assembly Language Translation - Part Two, by Michael Wimble. Part Two of this series examines statement scanning, label processing, intermediate text generation, building and organizing a symbol table, and op code processing. Subroutine flowcharts are used to illustrate the translation process 42

COVER THEME: Modular Program Design is represented by red and white blocks, presided over by the control module. This powerful approach to program design is detailed in the article beginning on p. 8. To the lower left is the four board Digital Group System shown plugged into the Standard Mother Board. This review begins on p. 35.

IMPORTANT NOTICE TO SUBSCRIBERS ON PAGE 29 (also see Publisher's Memo, P. 6)

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POSTAL NOTICE

MICROTREK, January/February, Volume 1, Number 2. Published bimonthly at 615 Guaranty Building, Cedar Rapids, Iowa 52401. Annual subscription rate for U.S., \$10; Canada, \$11; all other countries, \$12. Second class postage application pending at Cedar Rapids, Iowa 52401.

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MEMO FROM THE PUBLISHER

PERSONAL COMPUTING is a new and very successful publication in the small computer field. It is published by the Benwill Publishing Corporation of Brookline, Mass. Benwill is also known for DIGITAL DESIGN and other professional electronic publications. Effective with this issue, MICROTREK will have merged with PERSONAL COMPUTING. This simply means that articles and editorial which would normally be published and sent to you with the MICROTREK logo on the cover will now appear as a section in PERSONAL COMPUTING which, as a subscriber to MICROTREK, you will automatically begin to receive. The merger offers many important and immediate bene-

fits to our subscribers.

First, Benwill is an established publishing house with a reputation for getting their publications out on time. Benwill has long since mastered the tedious art of magazine production which seemed to defy our small MICROTREK staff with maddening persistence. Other improvements will appear in the quality, quantity, and graphic presentation of the articles. Full details of the merger appear on page 29 in this issue. Please note that PERSONAL COMPUTING is published bimonthly. However, with the conversion detailed on page 29, you receive more magazine (by page count) for your subscription dollar.

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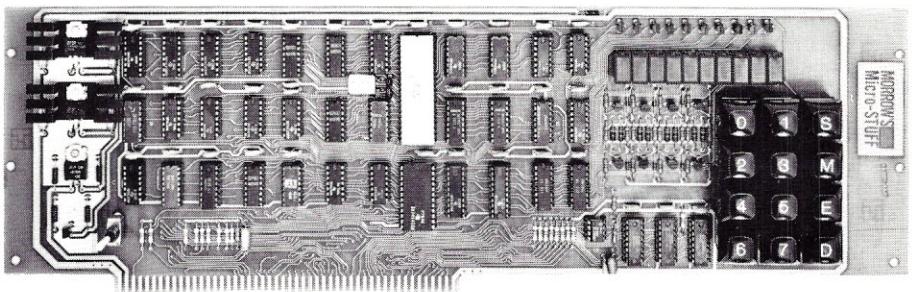
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modular

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by:

**Steve A. Hughes, Joe Celko,
and Elizabeth M. Hughes
5831 Hillside Drive
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The most difficult phase of programming is program design. For some programmers, arriving at a satisfactory program design is an intuitive process which can neither be readily explained nor taught to anyone who does not share the 'intuition'; but this is not the only, nor is it necessarily the best, approach to developing a program design. The remark of a professor of logic, that "There are two ways of solving a problem — you can have a sudden flash of inspiration or you can beat it to death," is just as applicable to program design as it is to logic problems (fig. 1). In fact, a rigorously systematic beat-it-to-death approach will often produce the right answer to a problem more rapidly than

the intuitive method, since an intuitive leap to a solution can easily overlook one or more important aspects of the problem.

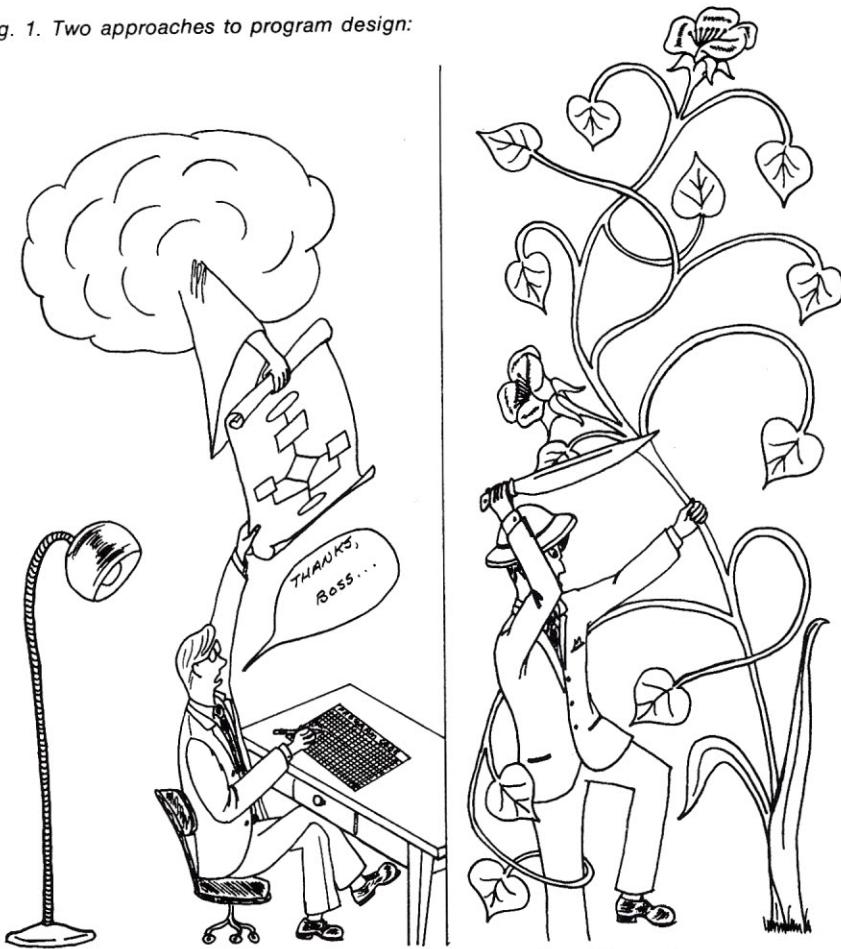
fear not

In this article we will present a systematic, non-intuitive process for developing workable program designs. Anyone can use it on any programming problem, small or large, simple or complex.

Many programmers of small systems, we have found, are overawed by some of the complex programs they try to create. They take one look at the apparent difficulty of programming a sophisticated game or some other application and decide not

to even attempt implementation. Frequently they start writing a program only to end up hopelessly confused by its complexity. Either way, they eventually give up and wait for someone to offer for sale a packaged program which will perform the desired functions. This is unnecessary. By adopting a systematic approach to program design, no programmer need shy away from any problem, regardless of its difficulty. Further, as systematic program design becomes 'second nature', design solutions take less time to develop. This process becomes almost intuitive, yet remaining more reliable than intuition, due to its uniform application to all problems and its certainty of

fig. 1. Two approaches to program design:



You can have a sudden flash of inspiration or you can beat it to death.

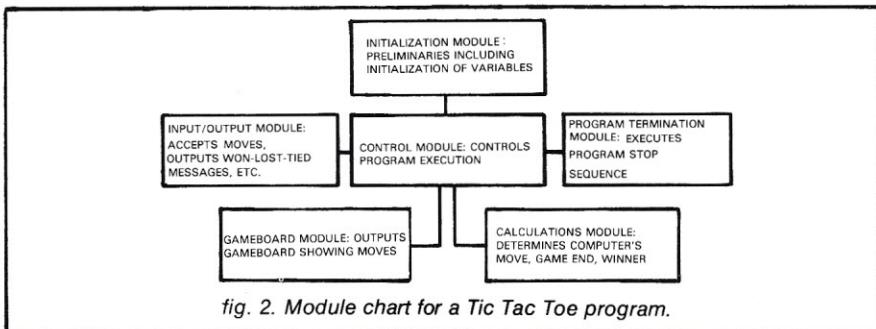


fig. 2. Module chart for a Tic Tac Toe program.

covering all the essentials of the problem at hand.

assessing I/O

The first step in any approach to program design is assessing the problem, deciding exactly what the program must do. One major consideration is the input and output (I/O), particularly in small systems where limited memory may pose a problem if a large amount of data is to be processed.

Let's consider the questions we will need to answer about I/O as an important part of sys-

tematic program design. What data will the program require and what will be its form? What information is to be output and what is the most useful format? If formatted output is desired (e.g., a gameboard or tabularized data), rough out the format on paper before attempting the program design. Use this opportunity to optimize the output format, reducing waste from unproductive hard-copy printout (to say nothing of reduced wear and tear on printers). Will there be output which requests input from the operator, such as ques-

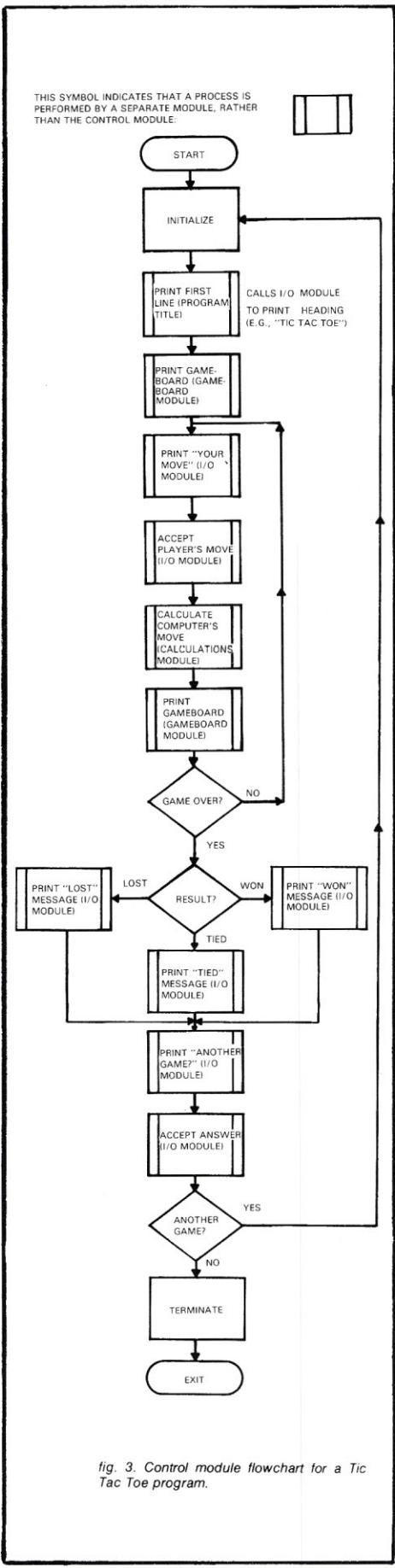
tions which the operator is to answer while the programming is running? If so, what is the exact form of the response which the computer will accept? Whenever a program is interactive, it is wise to indicate to the operator what the specific options and formats are for correct responses to computer interrogations; is "Y" or "YES" the correct response for Yes?

user convenience

A user will always do things the easiest way, and if using the computer program is more trouble than doing the job manually, he simply won't use it. Suppose a programmer writes a grocery-list program. He stores the Universal Product Codes for all available groceries, intending that his wife enter the quantity for each item as needed. The grocery-list program then directs the computer to print out the complete shopping list. Let's run through a hypothetical program run to spot the shortcomings of the program in terms of user convenience. First, each product is stored by its Universal Product Code. How many people know the Code by heart? Next, the program demands of us that if we do not want to order any quantity of a given product, we *must* enter a zero to indicate this. Imagine the time it would take to do this for each product available in the average supermarket! No one in their right mind would use such a system. The ease with which a program can be used will determine to a surprising extent its frequency of use; programs *must* be engineered for user convenience.

initial values

After the I/O format and options have been settled, the next consideration is to list the critical operations which the program is to perform. Making such a list will guarantee that



none are forgotten in the development of a complex program.

When the program variables and constants have been determined, initial values should be specified and any other preparations (such as I/O initialization, etc.) listed.

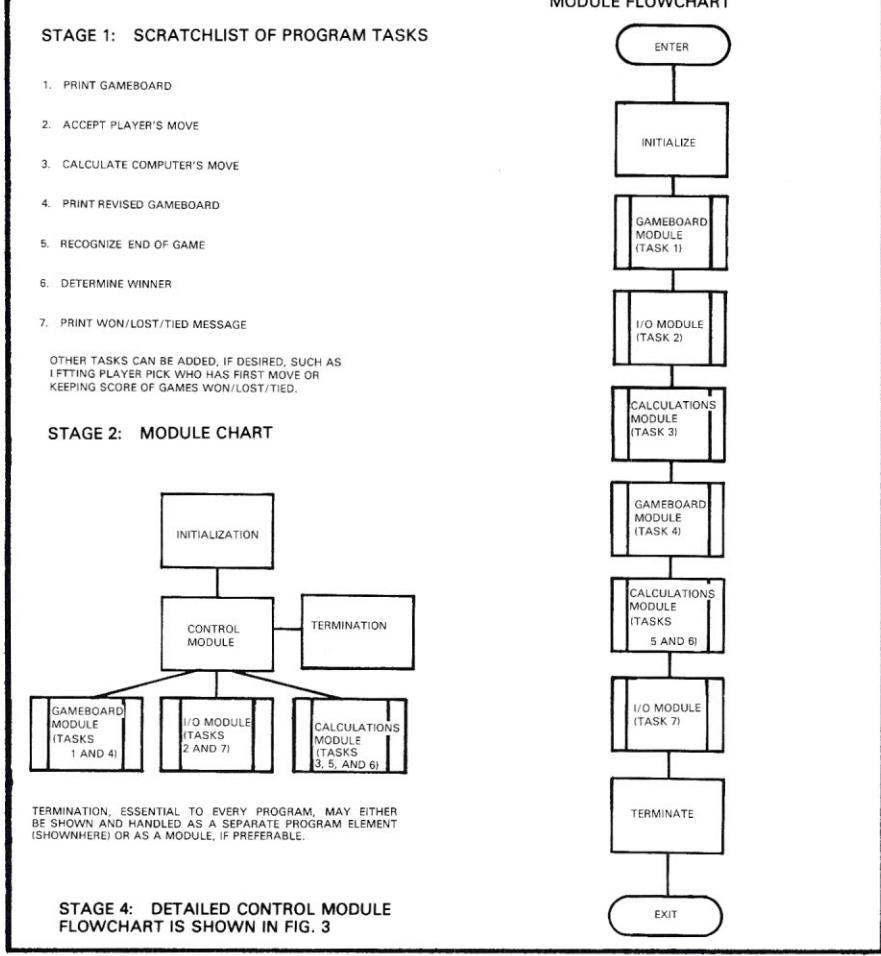
Tic Tac Toe program

To illustrate the process of systematic program design, let's consider how we might approach the design of a program to play Tic Tac Toe. We begin by assessing the operations which the computer is to perform. The program must output the gameboard, accept the player's move, decide what move to make and output the revised gameboard showing both moves. When appropriate, it must recognize that the game is over and declare a winner. Finally, it

must stop under program control.

The activities necessary to carry on the game of Tic Tac Toe can be grouped into related tasks. For example, one whole section of the program can be devoted to outputting the gameboard in its original and its revised states. Another task grouping would deal with accepting input and producing any output which is not a part of the game board, such as a prompting message to the player indicating the format of his play responses or the final won/lost/tied message at the conclusion of the game. A third program section is required for the calculations of the computer's best move and for the 'game over' determination. Formal program termination composes the final section of this or any other program.

fig. 4. The evolution of a control module.



program modules

As we have seen, the Tic Tac Toe program actually consisted of a relatively few task groups. Each of these tasks can be performed by separate sections of code which are brought into use by the main program as needed. The identification of these functional program modules constitutes an important part of the systematic method for program design. Almost every program includes I/O, calculations, and termination modules. In this particular game example we considered the task of outputting the gameboard separately, since it represents a different kind of I/O problem. This is the best approach in programs which must support an interactive environment which includes a television-type display.

module chart

The value of listing all the tasks which a program is to perform is that it shows clearly the modules which will be needed to create the program. Reducing all but the simplest programs to small, *workable* sections like these will always make programming go faster and with fewer errors. For the task list to be most useful, however, it should be sketched up into a *module chart*, which is the first (tentative) expression of the program design (fig. 2). A module chart identifies each of the functional sections composing the program and introduces the keystone into the program-edifice: the *control module*.

control module

A control module does exactly what one would expect: it controls the program's operation. The control module is responsible for the program's decisions and brings the individual modules which perform major program functions, like I/O, into play as they are needed. Perhaps the best (or at least the

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most amusing) analogy for a control module is the shepherd who kept "tuned sheep". Each sheep had a bell tied around its neck. When the shepherd tapped the sheep on the head with his crook, the sheep would nod its head, ringing its bell. By hitting the sheep in the desired order, the shepherd could play tunes. This is analogous to the

operation of a control module. It decides which operation is to be performed next (which note to play) and calls (hits) the appropriate module (sheep). The module (sheep) then performs the required operation (nods its head and rings its bell). This is the essence of the control module function; but since the control module must call all the

other modules as needed, its flowchart closely resembles a macro-flowchart of the program. On a module chart, the control module is shown immediately after the required initialization operations, and all remaining modules are shown attached to it (**fig. 2**).

Fig. 3 shows a flowchart of the control module for the Tic Tac Toe program, indicating the calling sequence to the function modules. This flowchart helps the programmer visualize the relationship between the control module and the other modules more clearly than the module chart, since it indicates at which points in the program's operation each module is called.

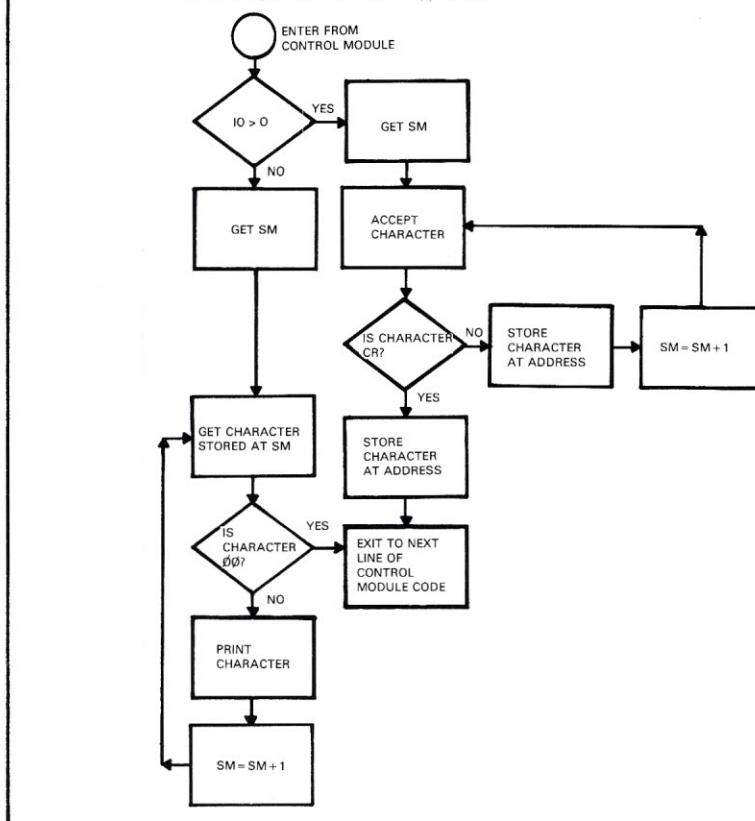
The control module is, as we have seen, the program's structure. Consequently, a well designed control module is half the battle in developing a good program. One of the advantages of using a modular approach to program design is that it reduces the apparent complexity of the problem to a minimum, allowing the programmer to concentrate on the essential details. This is particularly evident during the design of the control module, for it is here that the entire program is set up. If the data required for the operation of each module is completely defined, along with the required data formats, and the calling sequence is determined from the control module flowchart, design of the control module becomes a straightforward process. **Fig. 4** illustrates the evolution of a control module from the list of program tasks to the final form.

I/O module example

When the control module has been flowcharted, the programmer can begin to flowchart the individual function modules. **Fig. 5** shows the generalized I/O module flowchart. This module examines a variable (IO) to de-

fig. 5. I/O module flowchart.

VARIABLES AND SYMBOLS USED:
I/O = INPUT/OUTPUT INDICATOR (0=OUTPUT, 1=INPUT)
SM = START OF MESSAGE INDICATOR
FOR INPUT, CARRIAGE RETURN (CR) INDICATES END-OF-MESSAGE
FOR OUTPUT, AN ASCII NULL SYMBOL(00) IS USED



termine whether the operation required will be an input or an output. The module then finds the starting address of the message from another variable (SM). If the operation calls for data input to computer memory, the I/O module stores the first character it receives at the Start of Message address and the addresses which follow until it receives the *control character* (CR = carriage return) which indicates the end of the message or the conclusion of data. If, on the other hand, output is requested, the I/O module outputs data stored at the Start of Message address and following addresses until the end-of-message character is reached. Note that in either case, reaching the end-of-message character causes the I/O module to return control to the control module.

modules vs subroutines

In extremely simple programs, individual routines are used only once. A *routine* is simply a block of computer instructions (code) designed to perform a specific task. Thus, a program to average a set of numbers may treat the section which calculates the average as a single block of code; a routine. If however, the programmer wants to find the averages of several sets of numbers, the averaging routine must be repeated for each set of numbers to be averaged. To meet this need, he might employ a subroutine, since subroutines are an efficient method for dealing with code which would otherwise appear repeatedly in the mainstream of the program. A *subroutine* is a section of code which performs a specific task, which can be called into use by any part of the program. Once

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its task is complete, the subroutine returns control to the point in the main program from which it was called. Subroutines are designed to work on any variables they receive. This is an important point, as we shall see, and one which gives rise to the most infuriating bugs ever to plague programmers. If the wrong variable is somehow passed to the subroutine (arguments passed to subroutines are called "parameters"), the variable's value will change without the programmer's being aware of it. This error will most likely ripple through the entire program, causing further problems in the program's operation which can continue undetected until the programmer finds that his output is gibberish. The process of isolating and neutralizing this sort of bug is generally long and troublesome.

A module, on the other hand, is designed to avoid these difficulties from the start. Like a subroutine, a module is a body of code which performs a single task; and, like some subroutines, it has only one point of entry and only one exit. This means that whenever a module is employed, it starts at a well defined beginning, goes through a particular process to accomplish its task, and stops its activity at a single point. There is, however, an essential difference between modules and subroutines. The *only* variables which a module can change are those which it has been designed to use for receiving data from the control module and for making information available for other modules to use. This restriction completely rules out the possibility of its changing any *common* variable (i.e., one which can be accessed and used by more than one module) which is not *specifically* designated for its use. Within its own structure a module may perform operations on internal

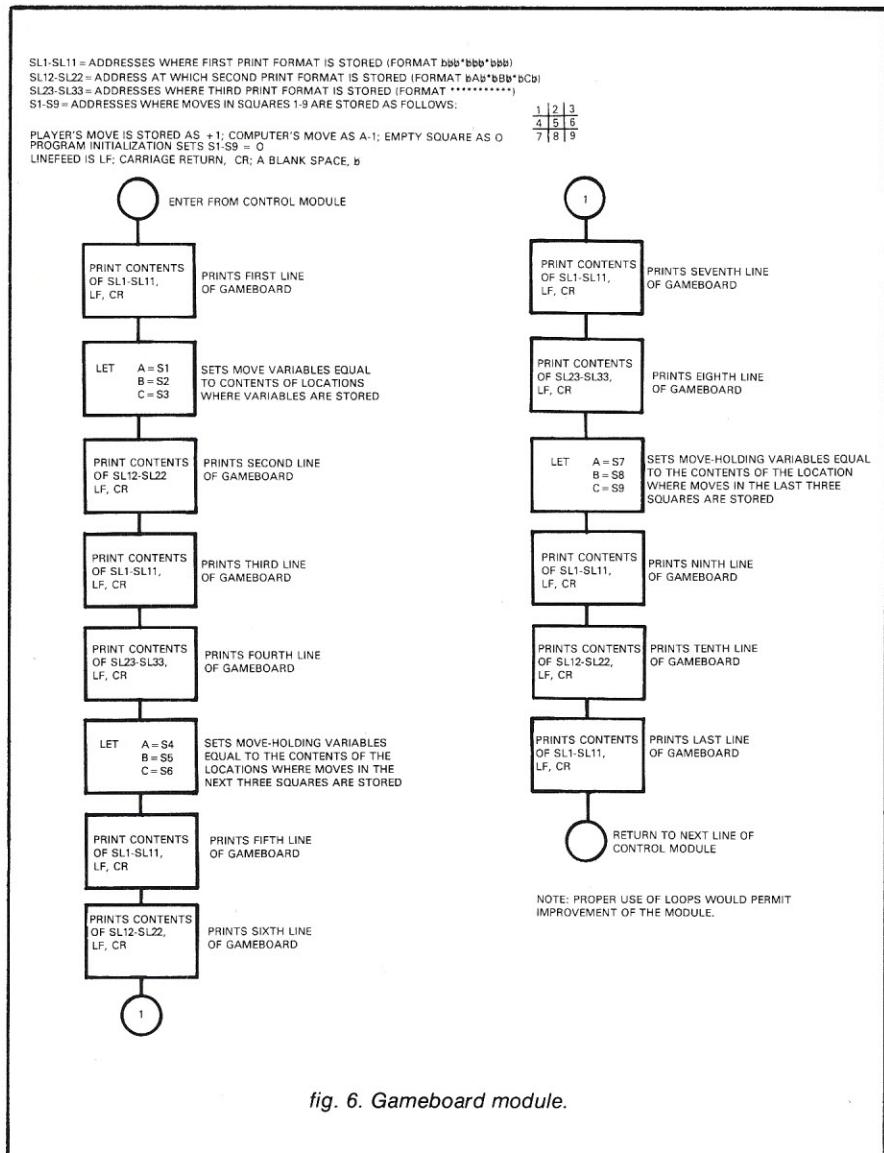


fig. 6. Gameboard module.

variables (called *local* variables), but since these variables will never appear outside that particular module, no mysterious catastrophic failures can occur.

linking variables

Returning to fig. 5, let's see how the I/O module operates according to our concept of modularity. First, the I/O module accepts and uses the variable called I/O, set by the control module, to decide whether it is to perform an input or an output operation; but it doesn't change the value of IO, and IO is only used by the I/O module and the control module. These two variables provide the sole link

between the I/O module and the rest of the program. With only these two links, there is little possibility of the I/O module spreading errors through the rest of the program. That, in a nutshell, is the advantage of modular programming. It also points out the care which must be taken in preparing the control module to assure that all common or "global" variables are in a form acceptable to any modules which use them. This is rarely difficult, however, since frequently only the control module and one other functional module will share some common variable. Also, the care required in establishing common variables is counterbalanced by

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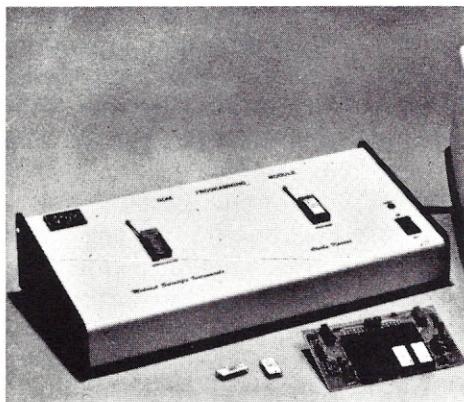
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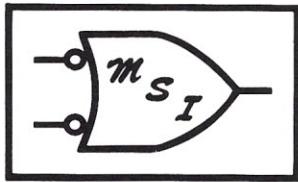
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the ease of establishing local variables, since a local variable only needs to be in a form suitable to the module which is its locale.

portable modules

Once modules are fully understood, the process of developing the remainder of the program becomes simple. After flowcharting the control module, the remaining modules should be flowcharted, especially if their operations are at all complex. The main consideration in flowcharting individual modules is to make them highly *general* from the standpoint of applications. This is done partially to avoid limiting the program's applicability in unnecessary ways and partially to make the module as portable as possible. A portable module can be moved from one program to another with almost no alterations if it is sufficiently general. This is exemplified by the I/O module discussed above, which can be used anywhere that an input/output module is required with few, if any, modifications.

modular modification

Two modules in the Tic Tac Toe program are tied to this particular game: the gameboard output module and the calculations module. **Fig. 6** shows the flowchart for the gameboard module. Note that only three different line-output formats are used to output the entire board, including the moves by both players at the various stages of the game. Although it is unlikely that many uses could be found for this module apart from the Tic Tac Toe game, it is easy to see how simple a matter it would be to modify it, if desired. This is yet another advantage of modular programming. Instead of requiring that the entire program be rewritten whenever an improvement or alteration is desirable, only the few modules

which affect the change need be modified and re-debugged. This means, for example, that should a programmer wish to modify his Tic Tac Toe program to permit play on a 4 X 4 board, he only need rewrite the gameboard and the calculations modules in order to implement the change. Further, since each module can be checked out independently of the other modules, the programmer could continue to use the original 3 X 3 game until he was ready to replace the two modules with their 4 X 4 versions.

calculations module

The calculations module, shown in **fig. 7**, is the one exception to the rule that modules should be generalized for portability; but since the main distinguishing feature of a program is its set of calculations, it is rarely either possible or desirable to move a calculations module from one program to another. It frequently occurs, however, that programmers discover improved ways of performing the calculations for programs which are up and running. When this is the case, a modular approach to a program's calculations earns its keep. The improvement can be incorporated into a new module, tested (by observing its output while the input is varied over the range of acceptable input values, including boundary values), and simply plugged into the original program which employed the former calculations module, without numerous bugs and similar problems commonly associated with an analogous substitution in a non-modular program. Whether the change is an improved calculations technique or an improvement in the game (e.g., a larger gameboard or the addition of a third dimension), the modular structure makes it easy to implement.

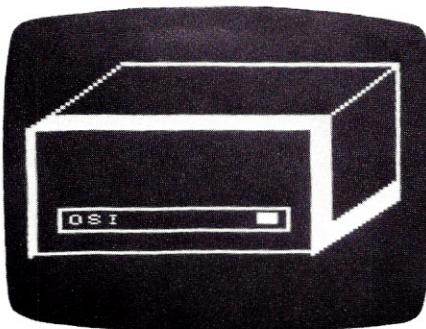
one step at a time

After each module has been flowcharted, it can be coded and tested independently of the rest of the program. Since, in order to write a module, it is necessary to know the form in which data is used by it, one can easily write dummy code which gives it test data in the correct form and outputs what the module would produce if it were connected to the rest of the program. Similarly, the control module can be tested by inserting dummy code at the points where it would call other modules (often a simple RETURN instruction will suffice). The remaining modules can be tested separately before being added to the program; or, after the control module has been debugged, they can be tested, one-by-one, from their actual positions in the program. In this way, the program can be built up in piecemeal fashion, with no more than one section of it needing debugging at any given time. This simplifies the debugging process, permitting the programmer to get his system up and running sooner than if the whole program had to be debugged simultaneously.

criticisms

Two disadvantages are occasionally advanced against modular programming, namely, that it takes more storage to run a modular than a non-modular program, and that it takes more time to write a modular program than a non-modular one. Both of these criticisms are misleading. If the time required for writing a program includes checkout and debugging time, modular programming is almost always much faster. It is easy to overlook debugging time until one actually has to debug a program, but the dramatic reductions in checkout time provided by modular program design more than compensates for any slight increase in the time re-

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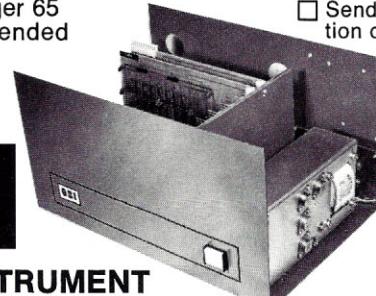
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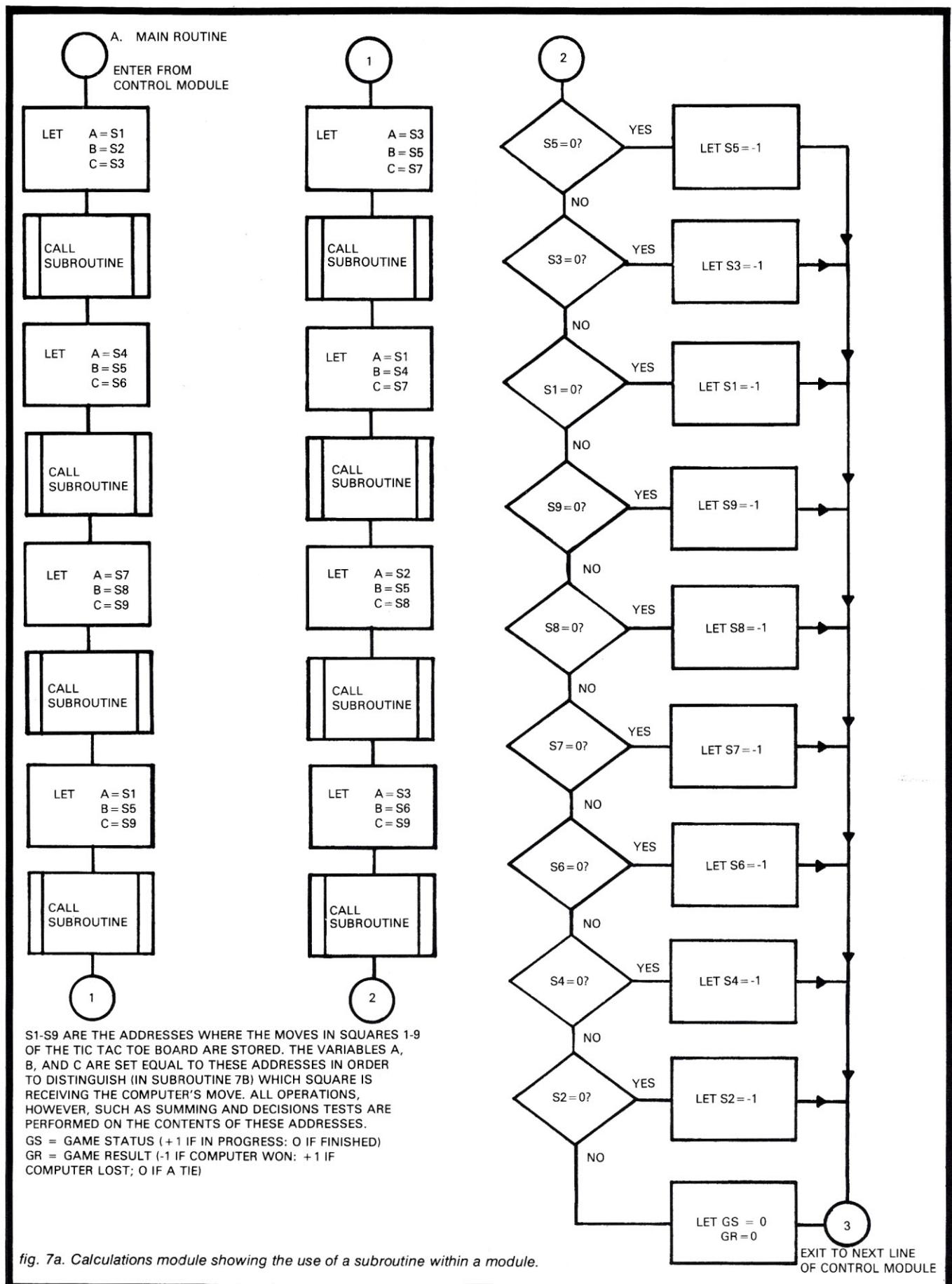
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quired to develop the original code. This is nearly always the case when a job is thought out before it is put on paper: the programmer who thinks it through may not start as soon as the one who just charges in, but he usually has less trouble with it and emerges with the right solution first. The complaint about storage is similarly ill-founded. Although the best

possible straightline program will usually take less storage space than the best modular program, for a given task, few programmers produce the best possible program for their problem with regularity. Given the normal programming conditions, modular design almost invariably requires less storage. An added benefit of modular programming on systems with

limited memory is that, if the whole program won't fit in the available storage at once, a module can be read in when it is needed, then read back out again, along with its local variables (onto tape or a disc memory) when it is not in use. This brings within the range of limited-memory systems programs which simply couldn't be run otherwise, since partial program loading of this sort is a sheer impossibility with a non-modular program.

conclusion

The approach we recommend for program design, then, is not only simple and direct, but applicable to any problem which faces the small systems programmer. The program design process can be summarized in a few statements:

- 1 — Assess the problem
- 2 — Divide the problem into single tasks
- 3 — Draw a module chart
- 4 — Flowchart the control module
- 5 — Flowchart the remaining modules

6 — Code and test the modules individually, assembling them into the complete program.

The result: a finished *working* program. Some extremely simple programs are best treated as single modules, but with any program of more than minimal complexity, going through the steps listed above will probably produce the quickest and most reliable solution. The next time you start wishing you could have a program that played some complicated game or handled an involved application, don't just wish — use our modular approach to divide and conquer the problem. Even the most awe-inspiring programs are easy to handle when they're divided into smaller, workable sections — and that's what modular programming is all about. **END**

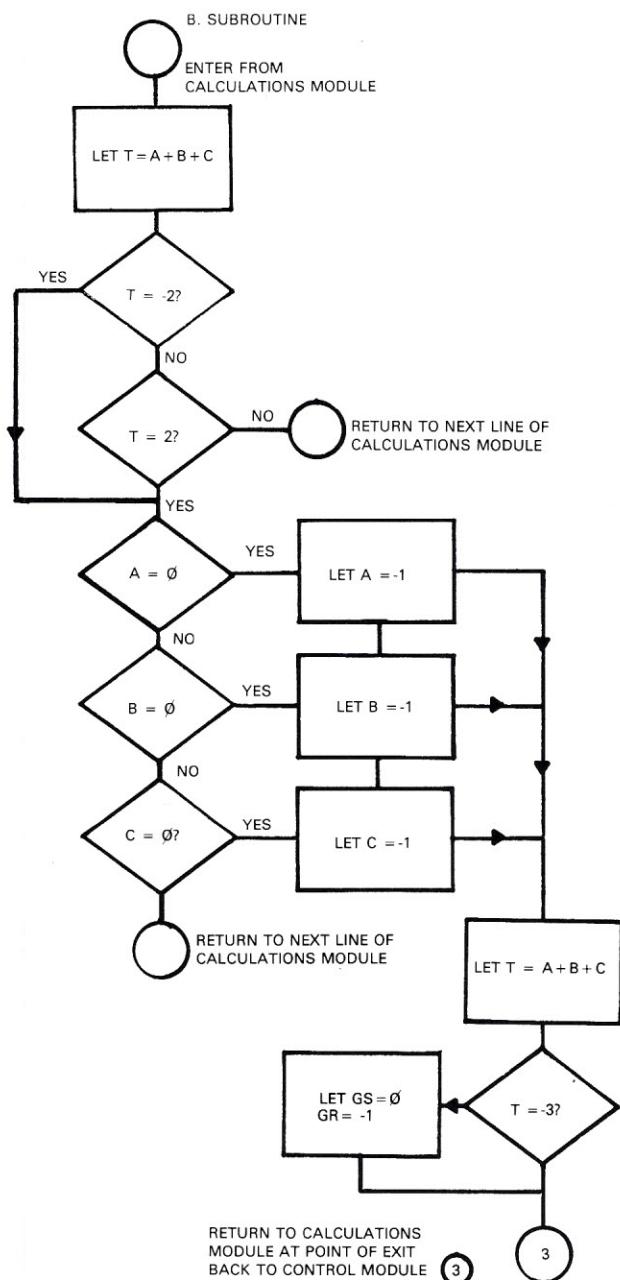


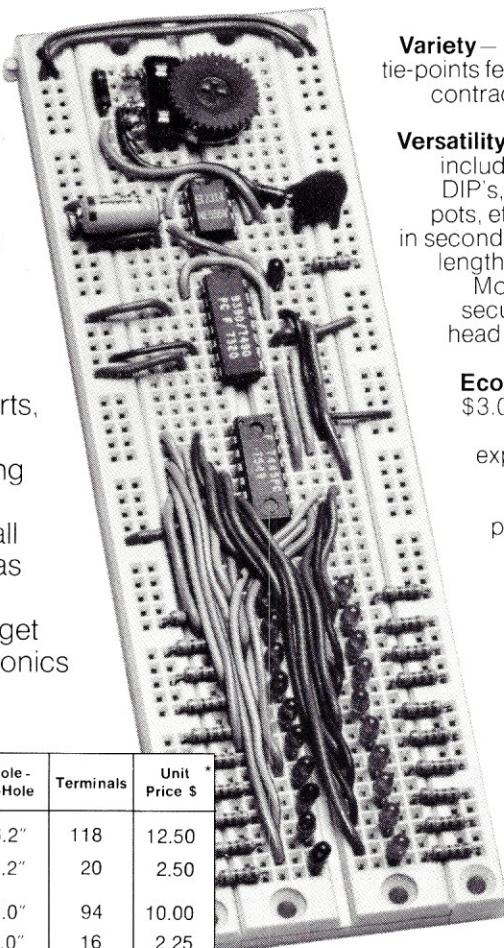
fig. 7b. Calculations module subroutine.

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interfacing

a microcomputer

to a pocket calculator

by Michael Wimble
6026 Underwood Ave. S.W.
Cedar Rapids, Ia. 52404

Originally, microprocessors were designed to emulate primitive minicomputer functions for service as terminal data handlers and industrial controllers. This is why microcomputers usually offer little in the way of built-in arithmetic functions. The recent emphasis on small computers offering high-level languages has created a demand for decimal arithmetic, floating point decimal, and trigonometric and statistical functions. Software implementation of these functions, although not necessarily complex, is usually tedious to develop, difficult to debug, and requires large amounts of expensive main memory.

calculator alternative

An alternative approach to software implementation of the desired functions is to interface the computer to a pocket calculator, thus providing a hardware extension at low cost. Before we consider the implementation of this technique, let's examine its deficiencies. There are two penalties. First, pocket calculators tend to be

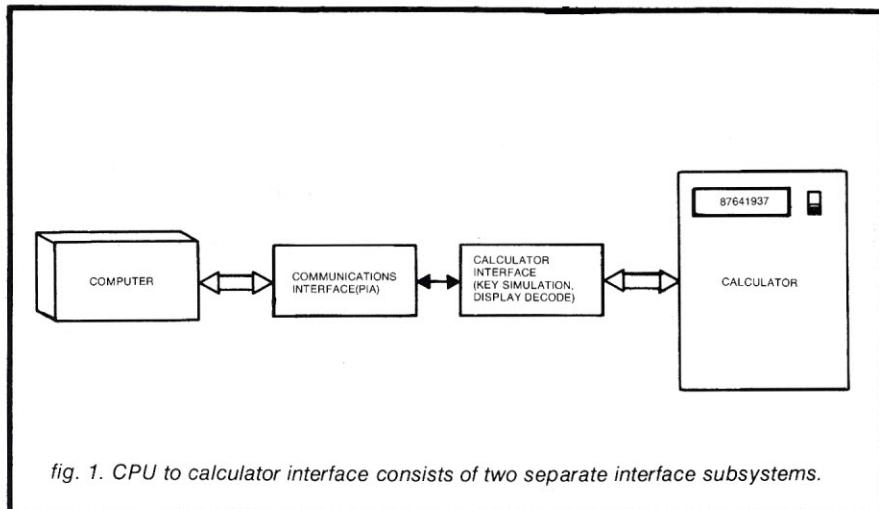


fig. 1. CPU to calculator interface consists of two separate interface subsystems.

table 1. Design goals for calculator interface.

1. The calculator is to remain useable as a pocket calculator. It must be designed to unplug from the interface for personal use.
2. Design requirement 1 and the need to develop a general interface which can be quickly attached to most popular calculators calls for an interface which will simulate keyboard entry.
3. The seven-segment calculator display is to be demultiplexed and decoded by the interface under computer control to provide addressable BCD digits for input to the computer.
4. All signal level-shifting required to connect the computer's communications interface with the calculator's keyboard and display are to be performed by the calculator interface.

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slow; some calculators can barely perform ten multiplications per second. This speed limitation is usually acceptable for small systems which are not operating in a demanding real-time environment. The second objection is that we must design a special interface to connect the calculator to the computer.

choosing the calculator

Calculator selection should be made on the basis of a realistic assessment of the expected results. Extended computational delays may prove to be an intolerable nuisance factor, even

Table 3. Definition of Port No. 1 bits 4-7 sent from computer to the calculator.

| PORT No. 1 bits | Definition of "enter digit" command | Definition of "enter operation" command | Digit addressed for "read display" command |
|-----------------|-------------------------------------|---|--|
| 4 5 6 7 | 0 | (not used) | digit 0 (rightmost) |
| 0 0 0 0 | 1 | ADD | digit 1 |
| 0 0 0 1 | 2 | MULTIPLY | digit 2 |
| 0 0 1 0 | 3 | DIVIDE | digit 3 |
| 0 0 1 1 | 4 | SUBTRACT | digit 4 |
| 0 1 0 0 | 5 | PERCENT | digit 5 |
| 0 1 0 1 | 6 | CLEAR/CLEAR ENTRY | digit 6 |
| 0 1 1 0 | 7 | (not used) | digit 7 (leftmost) |
| 0 1 1 1 | 8 | EQUALS | (not used) |
| 1 0 0 0 | 9 | DECIMAL POINT | (not used) |
| 1 0 0 1 | (not used) | (not used) | (not used) |
| 1 0 1 0 | (not used) | (not used) | (not used) |
| 1 1 1 1 | (not used) | (not used) | (not used) |

in a personal computing system. First, list the functions you will need. Then measure the delay required by your intended calculator subsystem, being mindful of accumulated delays resulting from repeated use of a slow function. Naturally, selection of a sophisticated calculator offering greater precision (and therefore more digit enable lines) and numerous functions (each operated by a separate keyswitch line) will increase the cost of the interface.

interface functions

Fig. 1 illustrates the relationship of the two general interface functions required to establish communication between the calculator and the processor. A *communications interface* typically consists of one or more PIA's (Peripheral Interface Adapters), one-shots, address decoders and buffers. This interface handles data transferred to and from the processor bus. Therefore, its design is highly dependent upon the specific processor to be used. Since this type of interface is commonly offered as a standard package with most small computers, its design will not be covered here. The calculator interface, on the other hand, is a

function of the calculator architecture and will be the subject of this article. Software routines for handling the data transfer at the computer side of the interface is also dependent upon the processor and the processor's communication interface. Therefore, software details will not be considered. It should be sufficient to point out that this software is much simpler than the arithmetic and trigonometric routines which we are replacing with the calculator and interface. Additionally, this software is primarily of the "LOAD and STORE" type and should be easy to write once the calculator is interfaced.

The following sections will discuss the design problems and hardware solutions will be offered. Information encoding and decoding, level shifting, and synchronization are covered. To aid in illustration of the techniques discussed, the specific example of interfacing to a simple five function Sears Roebuck calculator is presented. It is intended that the information presented will aid the reader when interfacing any of the popular

Table 2. Typical bit level definitions for 8-bit input and 8-bit output ports used in a practical CPU communications interface connected to the calculator interface.

PORT No. 1 — CPU TO CALCULATOR

| BIT | USE |
|-----|---|
| 0 | Read display |
| 1 | Enter command |
| 2 | Enter digit |
| 3 | (not used) |
| 4-7 | For "read display" command mode, bits 5-7 specify digit to be displayed. For "enter command" mode, bits 4-7 specify the command (Table 3), for "enter digit" mode, bits 4-7 specify the BCD digit to be entered (Table 3) |

PORT No. 2 — CALCULATOR TO CPU

| BIT | USE |
|-----|--|
| 0 | Error indicator (user defined) |
| 1 | Overflow indicator |
| 2 | Decimal point locator |
| 3 | (not used) |
| 4-7 | BCD (binary coded decimal) representation of digit addressed by the "read display" command |

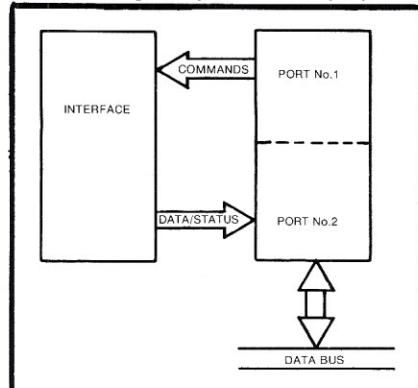


Fig. 2. Typical two port communications interface employing a Peripheral Interface Adapter (PIA).

fig. 3. Port communications example showing a typical enter and read sequence. Computer commands the calculator to perform 3.4×7 and reads result on an 8 digit calculator.

| PORt No. 1 | PORt No. 2 | MEANING |
|-----------------|-------------------|-------------------------|
| 0 1 0 0 0 1 1 0 | * X X X X X X X X | enter CLEAR command |
| 0 0 1 0 0 0 1 1 | X X X X X X X X | enter digit "3" |
| 0 1 0 0 1 0 0 1 | X X X X X X X X | enter decimal point |
| 0 0 1 0 0 1 0 0 | X X X X X X X X | enter digit "4" |
| 0 1 0 0 0 0 0 1 | X X X X X X X X | enter MULTIPLY command |
| 0 0 1 0 0 1 1 1 | X X X X X X X X | enter digit "7" |
| 0 1 0 0 1 0 0 0 | X X X X X X X X | enter EQUALS command |
| 1 0 0 0 0 0 0 0 | 0 0 0 0 1 0 0 0 | read digit 0(rightmost) |
| 1 0 0 0 0 0 0 1 | 0 0 1 0 0 0 1 1 | read digit 1 |
| 1 0 0 0 0 0 1 0 | 0 0 0 0 0 0 1 0 | read digit 2 |
| 1 0 0 0 0 0 1 1 | 0 0 0 0 0 0 0 0 | read digit 3 |

1 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 read digit 7 (leftmost)

*NOTE: X means bit value doesn't matter (not read)

pocket calculators with a general purpose microcomputer.

design goals

In order to insure that our interface will work with nearly every calculator on the market, our design goals (summarized in **table 1**) are to interface the calculator at the keyboard and display level. That is, our interface will appear to the calculator to be its keyboard, and the LED display control lines will connect directly to our interface.

I/O formats

Table 2 and **table 3** illustrate typical two port bit level definitions for the popular PIA type communications interface. The two port configuration is represented in **fig. 2**. Port No. 1 communicates information ("enter operation command," "enter digit," etc.) from the computer to the calculator. Port No. 2 communicates data and status information (BCD representation of the required digit, overflow indicator, etc.) from the calculator to the computer. **Fig. 3** shows a simple calculation transaction and the associated port data. The user should understand that it is the responsibility of the processor software to verify that valid data is sent to and received from the calculator. For this reason, bit zero of port No. 2 has been reserved for user definition

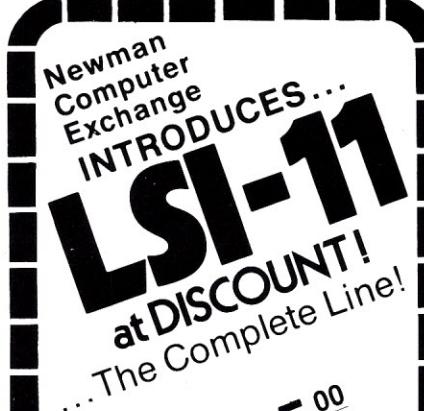
for error checking (which depends upon the specific type of error and display information supplied by the chosen calculator).

calculator interfacing

Fig. 4 shows the functional overview of a calculator for interfacing purposes. The keyboard is simply an array of S.P.S.T. switches whose closure is sensed by the keyboard scanning circuitry in the calculator. Output from the calculator consists of two groups of data lines; one group specifies which of the seven segments are to be enabled in order to form a digit, the other group selects the digit position which is to display this information. For example, to display the number "34" the display segments for the number "4" are first enabled and then the rightmost digit is enabled. This display multiplexing results in each digit being turned on and off several hundred times per second, appearing as a constant display to the human eye, in addition to saving considerable expense via component reduction and extending battery life.

keyboard interface

Different calculator chips employ different methods for obtaining keyboard input. However, it is usually the case that the keyboard consists of S.P.S.T. switches. A general in-



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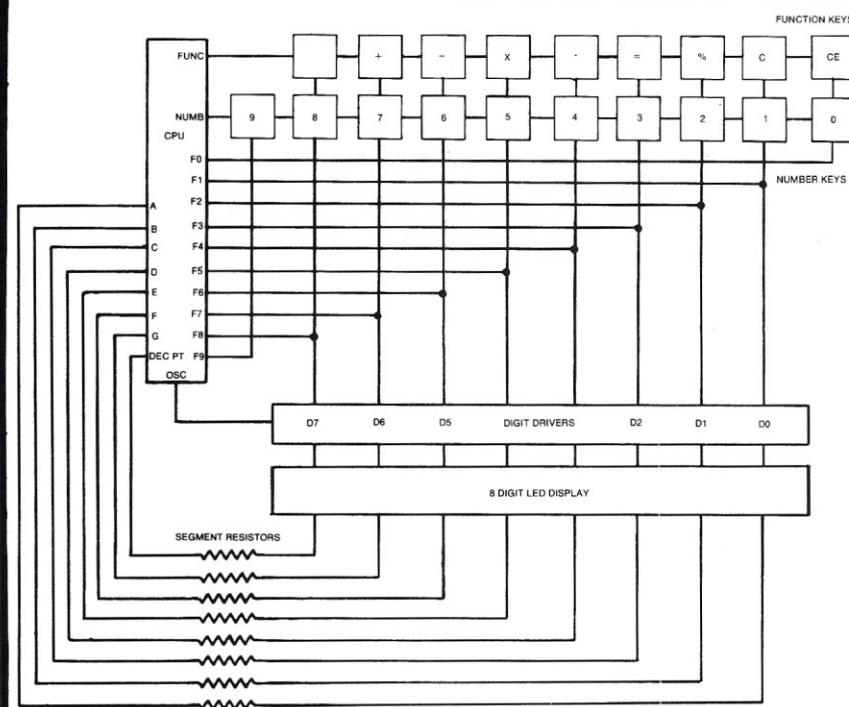
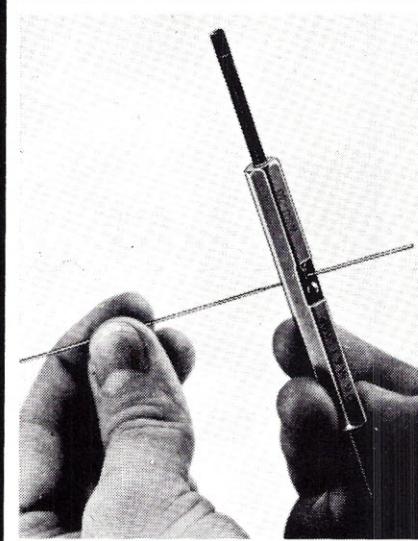


fig. 4. Functional overview of a pocket calculator.

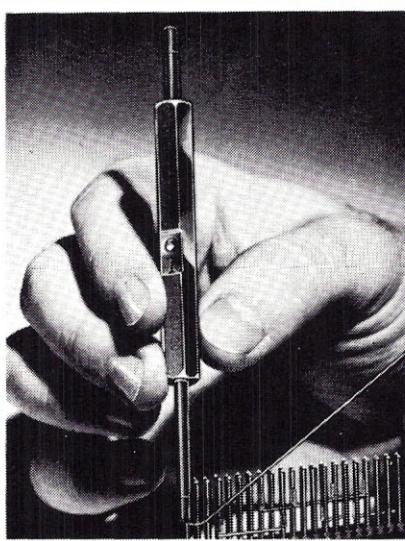
table 4. Relationship between keys pressed and keyboard connections shorted as determined with an ohmmeter.

| KEY | CONNECTIONS SHORTED BY THIS SWITCH |
|------|------------------------------------|
| 0 | f & l |
| 1 | a & l |
| 2 | b & l |
| 3 | c & l |
| 4 | d & l |
| 5 | g & l |
| 6 | j & l |
| 7 | e & l |
| 8 | h & l |
| 9 | i & l |
| . | i & m |
| + | a & m |
| × | b & m |
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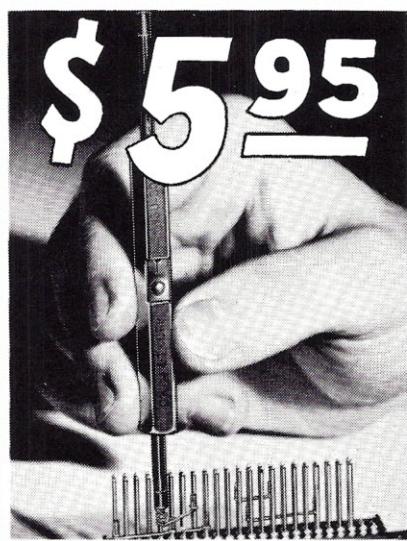
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terface can be implemented with only this knowledge by simulating keyswitch closure in parallel with actual keyboard keyswitches.

The first step is to determine the exact keyboard format used by the chosen calculator. One of three formats is commonly used:

1. Each switch is independent of all others, requiring two lines to be connected to each switch from the scanning chip or circuit.
2. The switches are diode encoded. There will be one *common line* for all switches and one separate line for each switch.
3. The keyswitches are scanned in multiplex fashion. This is the *most common* method and is illustrated in fig. 4.

If common lines are used in the keyboard configuration our interface circuitry will be simplified.

determining keyboard format

Like many inexpensive calculators, the calculator chosen for this article had a connector across the top of the printed circuit board which forms the contact panel for the keyboard. The cable connecting to the keyboard is shown as the righthand bundle of wires in **photo 3**. By labeling the keyboard connector pins "a" through "m" from left to right and using an ohmmeter, the relationships between keys pressed and connections shorted by these keys were determined as shown in **table 4**. As shown, there are two common lines employed (similar to the calculator shown in **fig. 4**). Line

"l" is common to all *digit* keys; line "m" is common to all *function* keys. Clearly, this type of keyboard is equivalent to two single pole, multiple throw switches. If this common line configuration is not present in your chosen calculator, it may be best to view the keyboard simply as a collection of independent S.P.S.T. switches.

device selection

There are many methods we could use to simulate the keyboard. Relays could be connected in parallel with the switches but the cost and board space required would make this a poor choice. In addition, transistor drivers may be required to activate the relays. Transistor switches could be used to simulate key closures.

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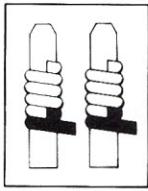
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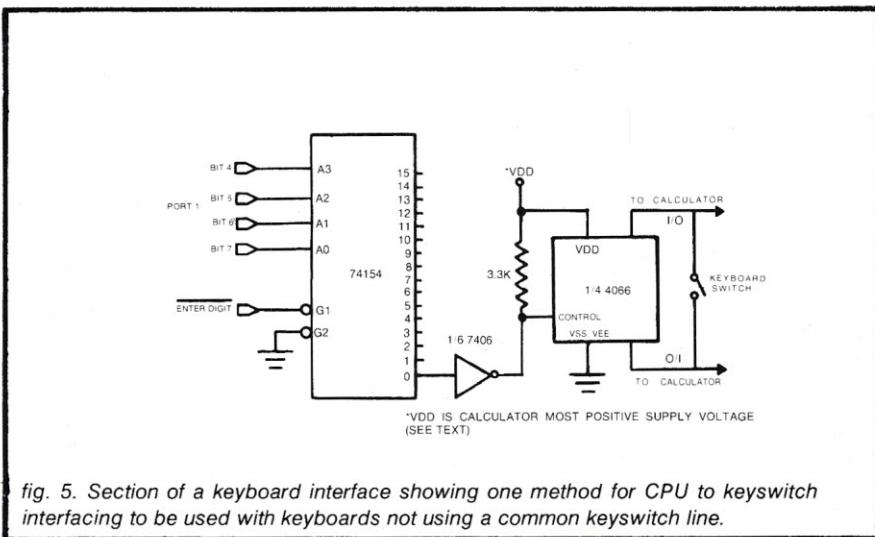


fig. 5. Section of a keyboard interface showing one method for CPU to keyswitch interfacing to be used with keyboards not using a common keyswitch line.

However, there is a better solution which is less expensive and more compact. The practical and least expensive method is to use the new CMOS analog switches. Several hobby supply companies are currently offering these for less than one dollar in quad (four units in one) packages.

level translation

Before we examine the CMOS analog switch as a simulation device for keyswitch closure, we must consider the problem of voltage level translation, specifically the translation required between the calculator and the CPU. The CPU generally communicates at TTL signal

levels, while the calculator may use one or more MOS voltage levels. If required, contact the *calculator chip* manufacturer to obtain pinouts and logic levels.

Do not feel that the manufacturer's recommendations must be blindly followed. In particular, shift the *relative* logic levels to a more suitable range if desired. If, for example, the calculator uses a +5V, ground, and -12V supply system, it may be more convenient to translate these levels to +17V, +12V, and ground. Notice that we haven't changed the *relative* logic levels with this translation. Establishing a frame of reference where all logic levels are positive with respect to ground simplifies the design of the interface.

transmission gates

The CMOS analog switch

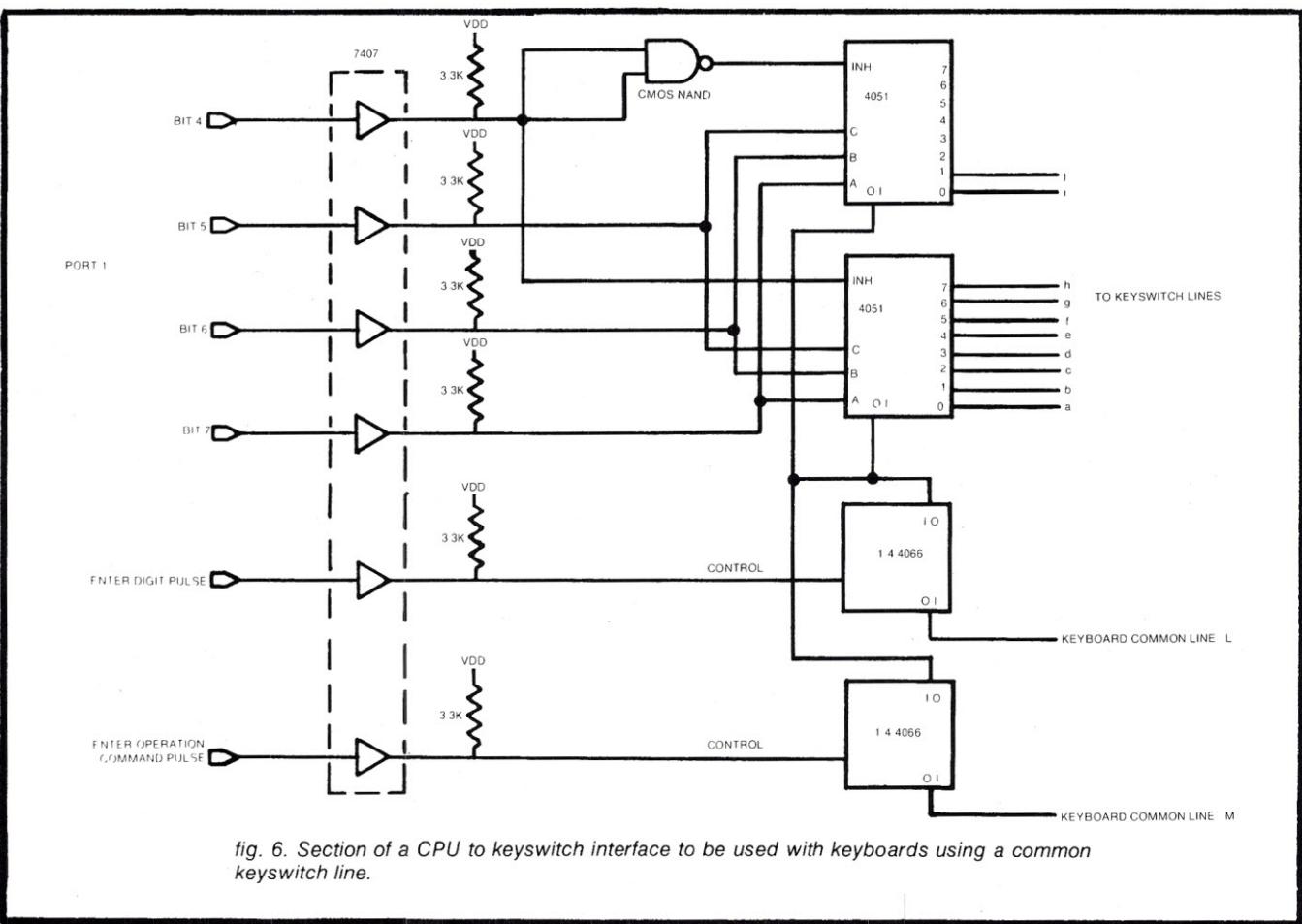


fig. 6. Section of a CPU to keyswitch interface to be used with keyboards using a common keyswitch line.

mentioned previously employs *transmission gate technology*. The gate is a solid state equivalent of a relay. When the control line is high, the gate will pass analog signals *bidirectionally* with very little resistance, typically from 80 to 150 ohms. When the control line is low the gate acts as an open circuit (10¹² ohms). The gate will, however, pass only those signals whose amplitude does not exceed its supply voltage. For example, if the gate is powered by a +5V and a -5V supply, then signals exceeding this range will be badly distorted. This is why it is wise to identify the most negative and the most positive supply voltages on the calculator chip and then assign the most negative level to be ground. All chip voltages will then be positive with respect to ground. If we connect the transmission gate to take its power between the level we have defined as ground and the most positive voltage on the chip, then we are assured that any possible voltage level present on the keyboard will be passed by the transmission gate and it will be able to simulate a keyboard switch.

The transmission gate power supply voltage levels determine what the control voltage must be in order to produce the desired "on" or "off" condition. In this article the control voltage for the "off" condition must be closed to ground, and the "on" condition requires that the control voltage be close to the positive supply voltage. By using a 7406 or a 7407 open collector gate, this level translation is easily achieved.

keyboard simulation

If the keyboard is organized as a collection of S.P.S.T. switches, CMOS devices such as the 4066 or the 4016 (similar to the 4066,

but has a higher "on" resistance and is less expensive) can be wired in parallel with the keyswitches. A partial interface employing the 4066 in parallel with a keyswitch which does not use common lines is illustrated in **fig. 5**. As shown, the 74154 4-line-to-16-line demultiplexer is used to decode the BCD digit lines from port No. 1 (review tables 2 and 3 if necessary). The "enter digit" pulse is used to enable the digit demultiplexer, causing the appropriate digit to be entered into the calculator. The 7406 converts the low going pulse to a high going pulse (since it's an inverter), and performs the desired level translation for the transmission gate. Since, as previously discussed, the transmission gate

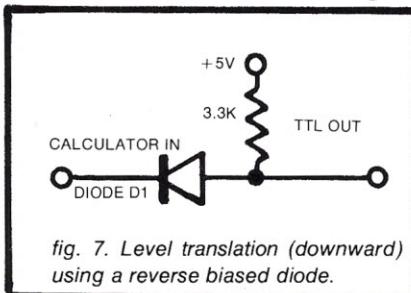


fig. 7. Level translation (downward) using a reverse biased diode.

takes its supply voltage between the most positive and the most negative chip voltages, the pull-up resistor on the open collector gate is used to raise the logic "1" voltage for the control gate past the threshold voltage.

common line circuit

Fig. 6 shows an interface for common line keyboards. The 4051 8-channel multiplexers select one of the non-common ("a" through "k") keyboard lines while the correct common line is selected via a 4066 transmission gate enabled from either the "enter digit" or the "enter operation command" line from port No. 1.

One final note about the keyboard interfacing circuitry; the "enter digit" and "enter

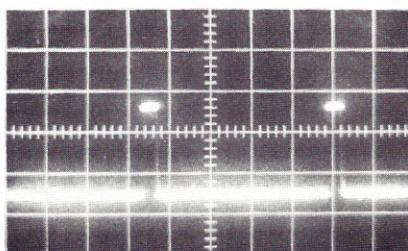


photo. 1. Waveform showing the digit and segment logic voltage levels for the calculator chip. Y=2V/cm, X=0.5ms/cm. Baseline is the bottom border of the grid.

operation command" lines must be pulsed to enter the information into the calculator. This is usually performed by a one-shot or similar circuitry in the interface. It may also be timed with a software loop. Some calculators may require that the enable line be low for some period of time before the next digit or command can be entered.

display interfacing

As nearly all the popular calculator chips produce the same type of output, interfacing to the display is more standard than interfacing the keyboard. Calculator results will be expressed as a multiplexed seven-segment code. Our interface must accomplish two goals: convert the multiplexed seven-segment information into addressable BCD information, and translate the calculator display control voltages to TTL levels used by the CPU's communications interface.

The downward voltage trans-

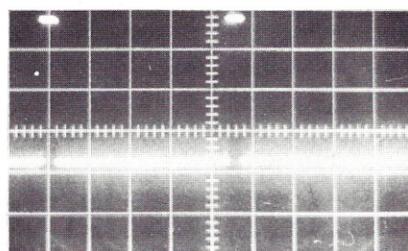


photo. 2. Waveform of logic levels in photo. 1 after passing through a CMOS NAND gate. Note that the baseline is the third grid line from the bottom.

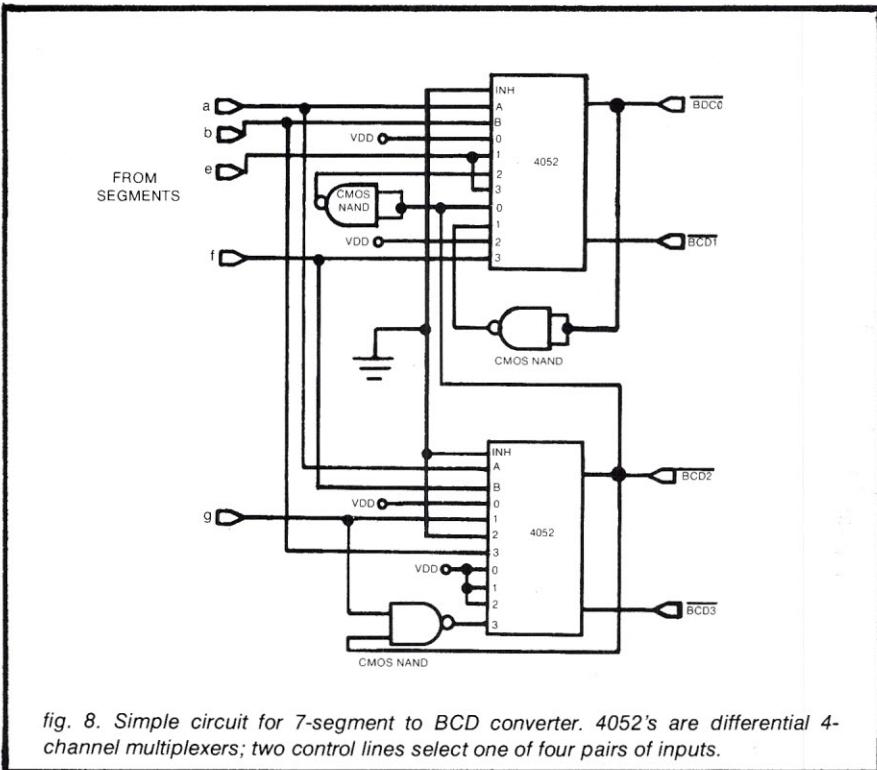


fig. 8. Simple circuit for 7-segment to BCD converter. 4052's are differential 4-channel multiplexers; two control lines select one of four pairs of inputs.

lation required at the display interface is at least as simple as the upward voltage translation required for keyboard interfacing. **Photo. 1** shows the digit and segment enable logic levels as they exist at the calculator chip. A logic "1" is about 7.2 volts while a logic "0" is about 3 volts. A simple resistive voltage divider could be used to translate these levels to the required TTL levels. However, this would also reduce the voltage margin between the logic levels, thus lowering the noise immunity.

Op amps could be used to provide a voltage offset to translate the logic levels while retaining the noise margin, but this choice would be expensive overkill and would require many discrete components. The simplest method is to use a reverse bias diode as shown in **fig. 7**. When the logic level illustrated in **photo. 1** is passed through this circuit, the diode clips the 7.2V level to the required 5V TTL level. The 3V logic level remains at 3V since the diode does not

clip at this low level. A TTL device would, of course, recognize this 3V level to be a logic "1" which it is not. In order to translate the input logic "0" level to the correct TTL level, we could simply pass the signal through a CMOS NAND gate. The result is shown in **photo. 2**; the logic "1" level is still greater than 7V, but the logic "0" is now 0.1V and will be recognized as a valid logic "0" by any TTL device. The 7V logic "1" is then passed through the diode circuit shown in **fig. 7** to translate this signal to a valid TTL logic "1".

7-segment-to-BCD

Rather than translate logic levels for seven 7-segment enable lines and eight (or more) digit position enable lines, it is more economical to perform the 7-segment-to-BCD code conversion first, and then to perform the logic level translation on the four BCD lines. There are several methods which may be used to convert 7-segment code to the BCD format but only one is recom-

mended here. NAND/NOR conversion is simple, but requires many IC chips. ROM lookup is ideal for those readers who have access to ROM programming facilities, but will not lend itself to a good solution for many hobbyists.

Fig. 8 shows a fairly simple and commonly used circuit for 7-segment-to-BCD conversion. The output of this circuit is passed through NAND gates to yield the previously mentioned logic level translation. The only remaining requirement for completing the calculator interface is to add the digit addressing circuitry.

Fig. 9 represents a complete display interface. The 4051 8-channel demultiplexer selects one of the digit enable lines to synchronize the conversion to the BCD format. Bits 5, 6, and 7 of port No. 1 give the digit address (as specified by the computer) and the "read display" line is raised. When the calculator display multiplexing circuitry pulses the appropriate digit enable line, the BCD data

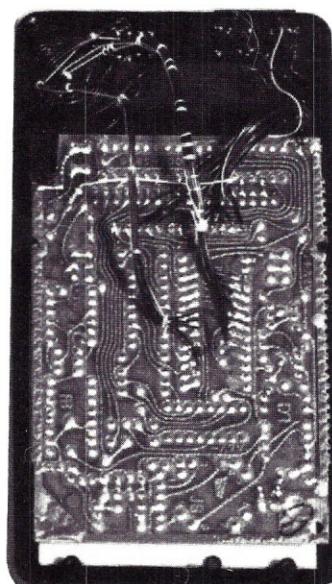
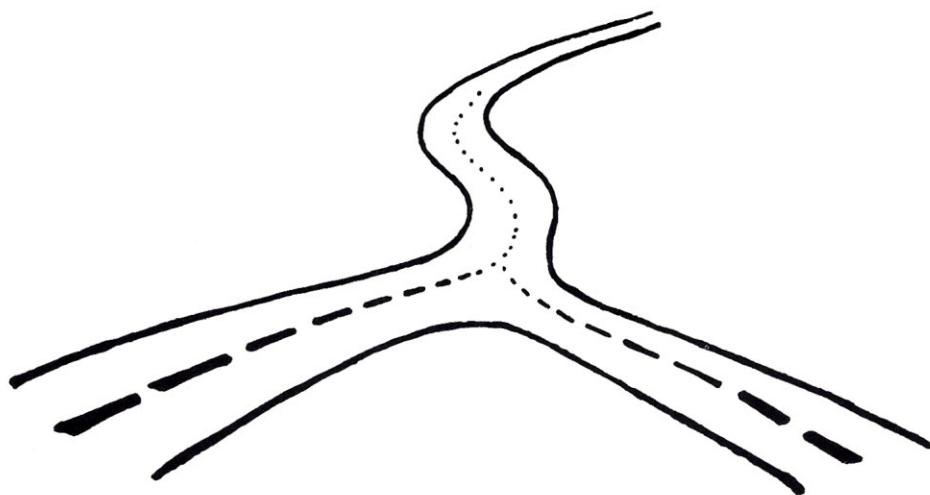


photo. 3. Shown in this photograph are the three cables used to interface to the keyboard and display.



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CASE 2: You subscribed to 14 issues of MICROTREK (offered on a limited basis at conventions) and have received 2, including this issue. You will receive 8 issues of the bimonthly PERSONAL COMPUTING (total value based on regular subscription rates to both magazines is \$12.32).

CASE 3: You have subscribed to both MICROTREK and to PERSONAL COMPUTING. In this case your subscription to PERSONAL COMPUTING will be extended to cover the merger issues plus your regular subscription.

PLEASE NOTE: If you have subscribed to both MICROTREK and PERSONAL COMPUTING, fill in your subscription numbers and name and address on the special card bound into this issue next to the inside back cover. Mail this card as SOON AS POSSIBLE to avoid any duplication in the issues sent to you. Use this card for any questions or comments you may have regarding this merger.

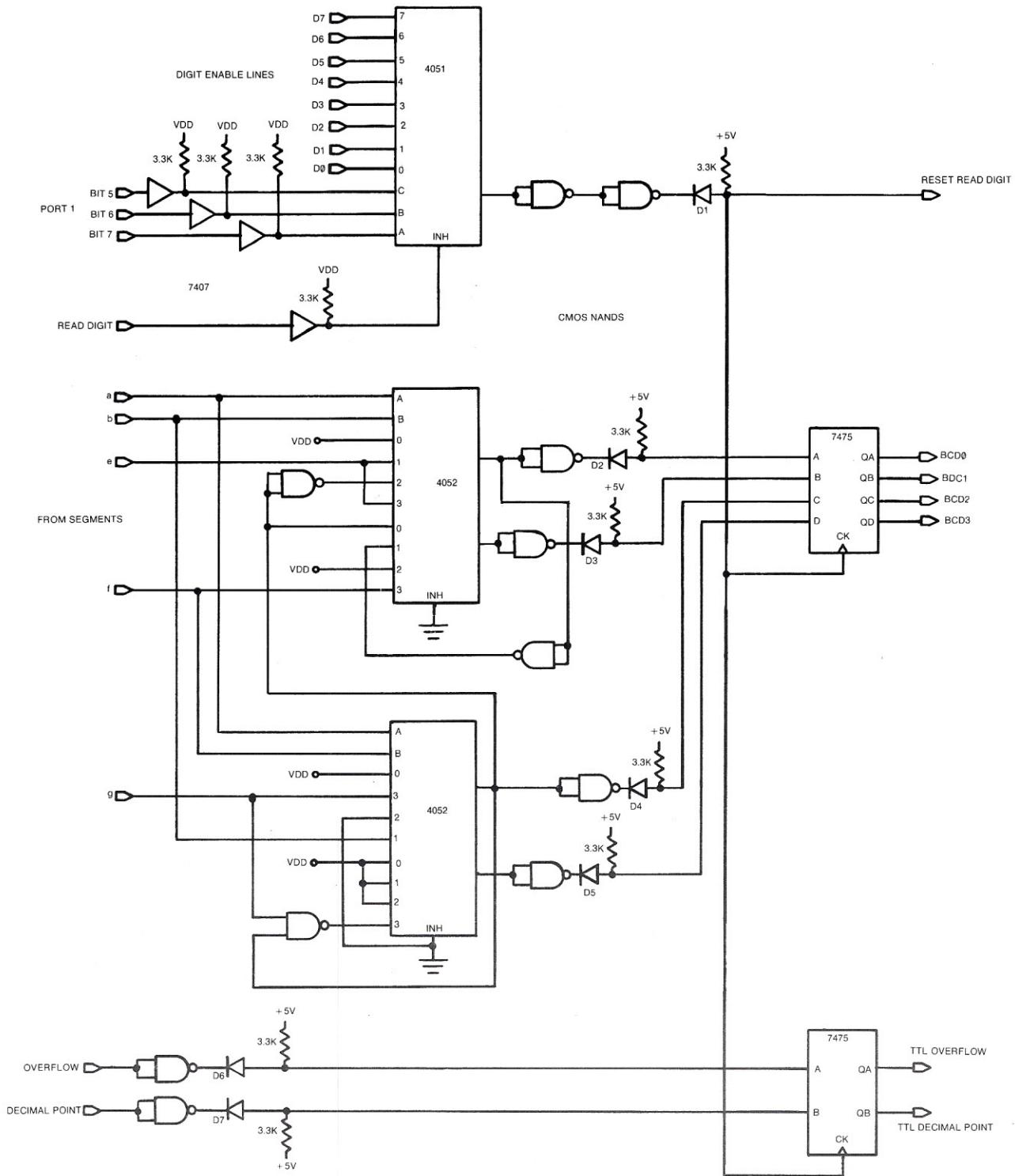
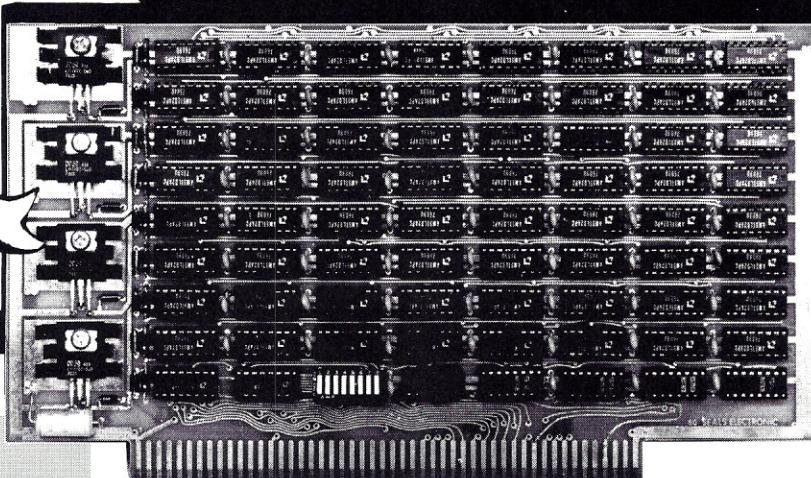
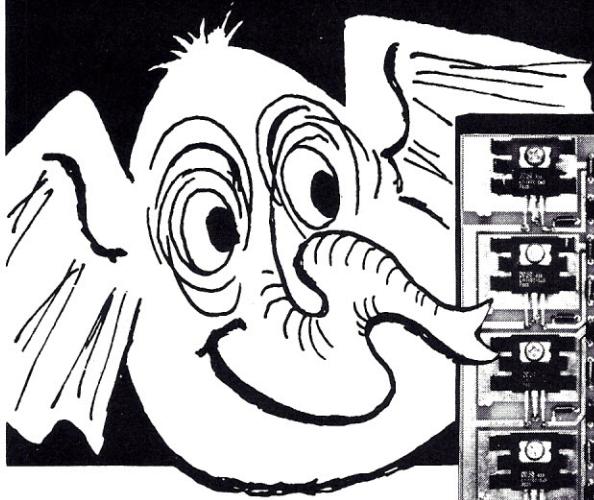


fig. 9. Complete calculator display interface with 7-segment to BCD converter, digit addressing (selects digit to be input to computer), and level translation.

The first 8-K that NEVER* FORGETS!



SPECIFICATIONS:

8K SC-8 Specifications:

| | |
|--------------------|--|
| Access Time: | 500 ns Max. (225 max on request) |
| Current Req: | Less than 200 ma per 1024 words maximum |
| Memory Chip: | AMD 91L02 APC (low power 1K x 1) |
| Voltage Supply: | +5 to +10 volts |
| Battery Standby: | 1.5 to 2 Volt, Automatic power loss sensing circuit. Eliminates need for switches. |
| Address Select: | 8 ea. Spst. switches in a Dip IC package. (No longer any need for a soldering iron to change address.) |
| +5 Volt regulated: | 4 ea. 7805 regulators with individual heat sinks to run cooler. |
| Wait States: | NONE! Your wait light will not burn because of a memory wait state. |

ALL ADDRESS, CONTROL, AND DATA OUT LINES FULLY BUFFERED

Circuit Board

Double sided, G10 glass epoxy board
Plated through holes. 5 mil. tin minimum
Solder reflow processed
Solder mask on both sides of PC board
Component lay out silk screened on
component side of PC board
Gold plated edge contacts
No jumper wires used
Professional layout techniques used

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PLUG IN-COMPATIBLE WITH ALTAIR® AND IMSAI®
IC SOCKETS INCLUDED

\$295.00 Kit — \$394.00 Assembled — \$2.00 Shipping and handling

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ELECTRONICS

BOX 11651, KNOXVILLE, TN. 37919

Enclosed is \$ _____ FULL AMOUNT 25%; BALANCE C.O.D.

BANK AMERICARD/MASTER CHARGE #_____

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8KSC KITS @ \$295.00 each
 8KSC ASSEMBLED @ \$394.00 each

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STREET _____

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The first complete small computer.

As you thumb through this magazine, you'll see a lot of ads for small computers. For \$600 you can find a pretty good box with a power supply, four slot mother board, CPU module, and all the expected lights and switches.

But you know what? It won't work.

That's because in order to make the computer go you have to buy memory—normally both read-write (RAM) and read-only (PROM), interfaces to the outside world (parallel, serial, and cassette), keyboard, video display module, and software.

Add this all up and it's going to cost you at least \$1,400 for a complete system.

Got the picture?

Now listen to this. The remarkable new Sol-20 Terminal Computer will give you all of the above... plus more!... as standard equipment for just \$995, in kit form. This is because the Sol-20—like no other small computer—was designed from the ground up to be complete.

Here's what the Sol-20 includes as standard equipment:

- 8080 microprocessor.
- Video display circuitry.
- 1024 words of static, low-power RAM.
- 512 words of preprogrammed PROM.
- Custom 85-key solid-state keyboard.
- Audio cassette tape interface.
- Both parallel and serial interfaces and connectors.
- Power supply.
- A beautiful case with solid walnut sides.
- Software that includes a preprogrammed PROM personality module and a cassette with BASIC-5 language plus two sophisticated computer video games.
- Full expansion capability with all S-100 bus (Altair/IMSAI/PTC bus) products.

It's a handsome terminal or computer that will even look good in your living room or office. Small systems start at just \$475.

Full expansion capability

The Sol-20 system can be tailored to your applications using the complete line of peripheral products from Processor Technology. These include the video monitor, audio cassette and digital tape systems, dual floppy disc system, memories, and interfaces... plus all other peripherals compatible with the S-100 bus.

The Sol-20 greatly simplifies the computer-buying process. It's a splendid package that will excite both present and prospective computer owners.

Our brochure tells all. Write for it today.

Processor Technology, Box P,
6200 Hollis Street, Emeryville, CA 94608.
(415) 652-8080.



The Sol-20 expandable system.



photo. 4. 16 pin DIP sockets mounted on the calculator case.

generated by the 7-segment-to-BCD converter is latched into the 7475 quad latch and a pulse is generated to reset the "read display" command line, assuring us that the digit is converted only once. This reset pulse may be sent back to the computer via an unused PIA line or it can be used with a one-shot to activate a hardware reset. The choice depends upon the particular communications interface used with the computer.

error flags

Other enhancements shown in **fig. 9** include capturing the decimal point and the overflow indicator. The decimal point indicator may be read directly from the chip. The overflow indicator may have to be decoded from the display for some types of calculator chips.

interface mechanics

Having discussed interfacing methods for both calculator input and output, there remains the details of the physical implementation. First there is the matter of interface connectors. Our goal of being able to use the calculator as it was originally

intended requires an interface connector which may simply be unplugged from the calculator.

Photo. 3 shows the three miniature cables used to connect the calculator to the interface sockets. The larger cable at the upper right contains the keyboard lines and the power supply leads. The center cable consists of segment enable lines, while the left cable contains the digit position enable lines.

line was routed through the interface sockets so that a shorting plug can be used to disconnect the calculator supply, eliminating any problems with power supply conflicts. When attached to the interface, the calculator is powered by the computer or interface supply and when the shorting plug is inserted, the calculator is powered by its internal batteries.

Do not assume that a 6V or a 9V battery pack means that the calculator actually runs at 6V or 9V. The sample calculator uses a 4V NiCad battery pack to supply a 7.8V chip voltage via the DC-to-DC converter in the calculator.

prototype interface

The interface prototype constructed by the author is shown in **photo. 5**. This interface contains a seven-segment decoder, display, and current limiting resistors on the upper right-hand portion of the board to display the contents of the 7475 quad latch. This makes it easy to check for correct digit addressing and to verify that the 7-segment-to-BCD conversion was performed as expected. This built-in debugger is especially helpful when developing the software to operate the interface.

Unless you have access to information detailing the logic levels and operation of the calculator you have chosen to use, I suggest that you prototype your interface with wire wrap sockets; it's hard to determine for certain if your interface gate is going to work with the calculator without exceeding its drive capabilities until it is actually tried. In addition, long connecting cables may cause ringing problems. The pocket calculator interface should prove to be an interesting and useful addition to your computer.

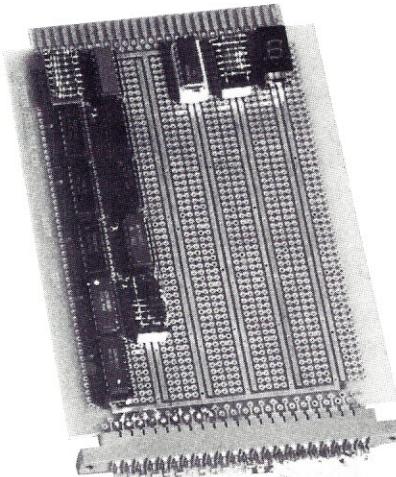


photo. 5. Author's prototype interface with built-in digit display for debugging.

As shown in **photo. 4**, DIP sockets were mounted on the top of the calculator case which was drilled to pass the cables. These 16 pin sockets were simply glued to the case. With this method very little space will be consumed by the interface connections.

power considerations

The calculator battery power

buyer's report:

the Digital Group System

by Steven R. Woodall
34 Fendale St.
Franklin Square, N.Y. 11010

"It plays the *Star Spangled Banner* on the radio while it draws a picture of the U.S. Flag on the TV," I argued. "We can't afford another expensive gizmo," countered my wife sharply. "And besides, it's a lot cheaper to watch the Bicentennial Minutes," she added. We were, of course, discussing the merits of my proposed purchase of a Digital Group (DG) System computer. Being a confirmed computerholic, I hocked my camera and bought the full-blown DG Z-80 system despite domestic objections.

Anything that pays for itself makes sense to me. That's why I chose the Z-80 version of the DG system (they can sell you just about any CPU board you might wish for). The additional cost of

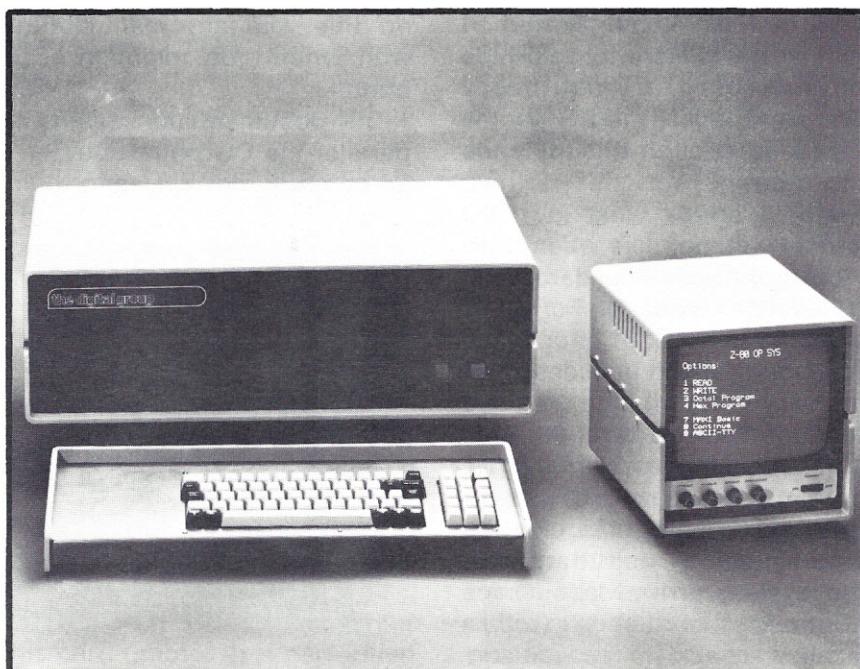


photo 1. The complete Digital Group System housed in distinctive tan and black cabinets. Promised shipping date to customers is early February.

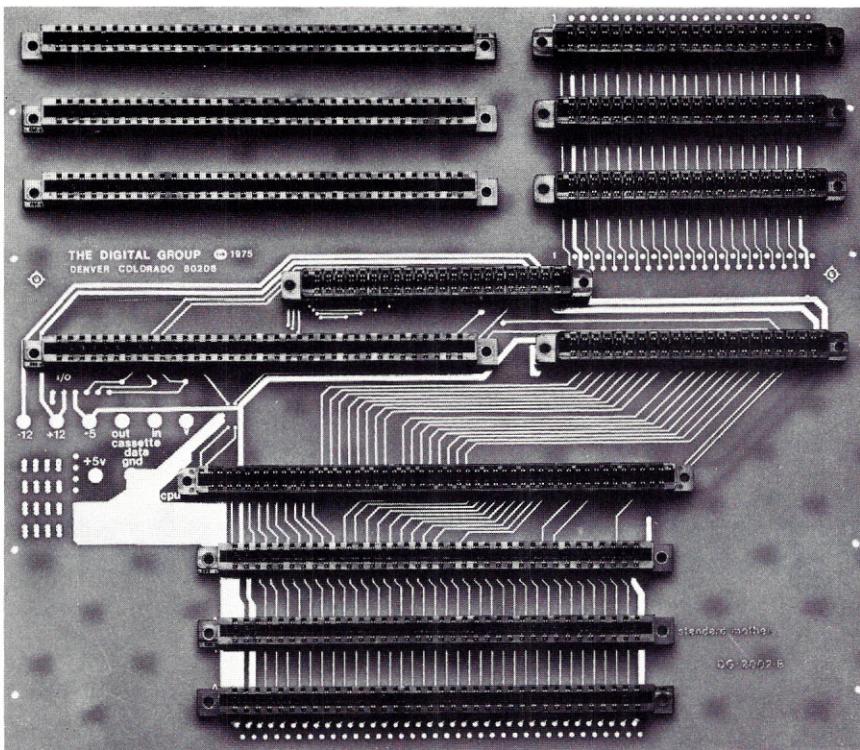


photo 2. This is the Standard Motherboard. It supports 26K of memory, 16 input ports and 16 output ports, in addition to the CPU, TV/Cassette cards.

the Z-80 CPU version is offset by the reduction in memory used by this super powerful chip. So there, 8080 fans — may the Bird of Paradise eat your 8228 system controller.

Since, as I mentioned, I hocked my camera to help hide the true cost of my new hobby from my spouse, the DG people were kind enough to supply the photographs for this article. **Photo. 1** shows what my CPU cabinet will look like when it arrives (promised ship date from DG is late January). For \$895 (shipping included) I bought the Z-80 board (which includes 2K of memory), an I/O card, TV Readout/Cassette card, 8K RAM card, 12 Amp power supply, Standard Motherboard, Standard CPU cabinet, fan, binder, documentation, and hardware. The system arrived about one month after I ordered it (with a certified check to reduce delays). If you have a pressing need (or can't stand suspense),

call the DG (303-777-7133) and get the current estimated shipping dates. I have found them to be exceptionally forthright and courteous. Call and get acquainted — and I suggest you do this with any manufacturer with whom you might invest a bundle.

DG documentation seems to parallel the DG philosophy — it is concise, correct, and com-

plete. It's not a dissertation on microcomputer theory, but it tells you what you need to know to put the system together and get it running. Each board is documented in a separate section which is well written and very carefully organized. My only objection is that the few component value corrections which show up in the documentation might have been noted in the very first part of the documentation. Detailed board debugging is included.

Since the motherboard embodies the character of the entire system, we will evaluate this board first. Incidentally, the order in which we will examine the boards is the assembly order recommended by the DG.

the Standard Mother

Photo. 2 shows the 'Standard Motherboard' fully populated with the appropriate edge connector sockets. Since each board kit comes with the required socket to mate it to the motherboard, the Standard Motherboard is supplied bare. Molex connectors are recommended for slipping over the wire wrap sockets supplied with each I/O kit to connect the input and output ports to peripherals. These are *not* included with the kits since the number of connec-

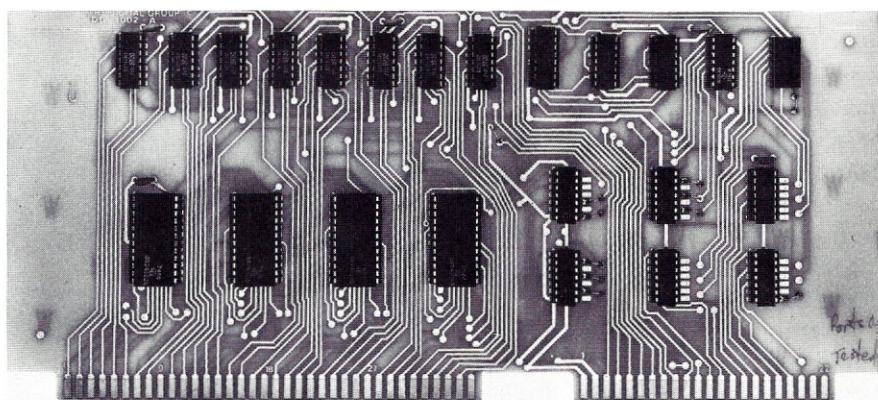


photo 3. Four latched 8-bit output ports and four gated (open collector to bus) 8-bit input ports reside on this board. Address jumping permits addressing these ports at any four consecutive locations in the 65K range.

tors required depends on the number of I/O ports you wish to establish. For \$35 you can buy a Molex connector kit, complete with flat cable, from the DG. Add \$8.95 if you need the crimp tool. Refer to the DG Flyer No. 5 for details regarding the Molex connectors.

I/O Card features

The DG I/O card is not a fancy programmable type. Instead of inscrutable Peripheral Interface Adapters (the title is bigger than the chip), we find a simple, respected workhorse — the 74100 TTL latch — serving as the output port element, and the even simpler 7404 open-collector dual-input NAND functioning as the input port element. That's what I like about the DG design; it's so simple that you will understand it even when it doesn't work. If you've ever had to trouble-shoot some of the complex, kludgey systems designed by people who worship large-scale integration circuitry, you will be soothed by the shocking simplicity of the DG system.

Address lines terminate in 16 7404 gates which are in turn connected to 16 7404 gates. This series buffer configuration permits the user to pick off the inverted or non-inverted address line signal for the desired decoding. The four 8-bit input and output ports on the I/O card can be set up only as a block of four sequential (contiguous for you picky folks) locations; 0-3, 4-7, etc. Here's the procedure: determine the number of the highest port to be on the card. Then find the combination of the powers of 2 which will add up to this number. For example, if ports 24, 25, 26, 27 are the ones you want, figure that 27 is a binary 11011. Therefore, tie the address straps No. 0, 1, 3, 4 to logic one pins (next to the in-

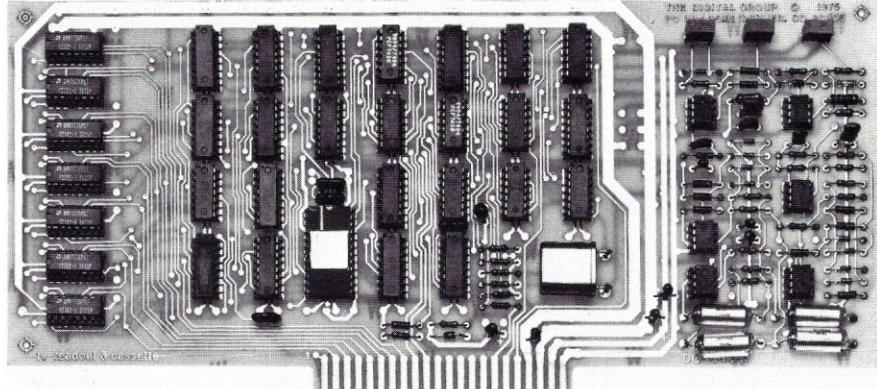


photo 4. Here we have the TV Readout/Cassette card. The readout employs a 7 X 13 dot matrix to produce each character for enhanced resolution. The display buffer consists of the RAM at the left, while the cassette interface active filter is on the right.

verter chips), and strap No. 2, 5, .., 15 to logic zero pins. All four ports are now properly decoded. And if this isn't simple enough for you, the DG documentation has a map of the straps with an example to make sure you understand how easy it is to set up the addressing.

Photo. 3 reveals the clean, open layout which should make it a snap for you to construct. I spent only a few hours on this board and it worked right off. Just remember to mark the card so you won't put it into the wrong slot — each I/O card is of course given a unique block of addresses, and the external connections to I/O devices are wired to these specific I/O slots.

TV Readout/Cassette card

Since all address decoding for this card (**photo. 4**) is performed on the I/O card, the DG decided to combine both the TV readout and the cassette interfaces on this single card. We will examine the TV section first.

Getting to the point with minimum frills sums up the DGs' approach to card-level design. The simple but effective circuitry of the TV Readout is a good illustration of the reliable, low-cost character display which results from the implementation of this philosophy. Exotic functions

such as reverse lettering (black letters on a white background) are not included, but a full range of upper and lower case ASCII characters, math symbols, Greek letters, and special symbols make this a very capable display for general programming and text editing (DG offers a Text Editor Cassette for \$7.50).

An unusual feature in this TV typewriter is the hardware Write position counter. This controls the location of the next character to be written on the screen. Casting this function in hardware permits the use of this display with any ASCII encoded keyboard in a stand-alone mode, freeing the processor from the chore of character writing to the display buffer. If, on the other hand, software control of the cursor is desired, character positioning becomes cumbersome because the Write counter must be stepped until the desired location is arrived at. Incorporation of a circuit to preset the Write counter directly from the processor would overcome this objection nicely.

A 2N5129 video combiner provides a composite video signal (3V p-p) which may be coupled into a commercial monitor, a TV set modified to serve as a monitor or a simple modulator/oscillator circuit for use with an

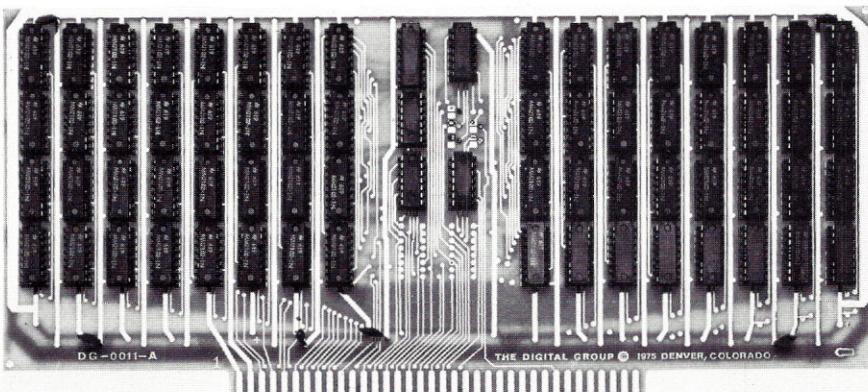


photo 5. The 8K RAM board shown here takes about four hours to assemble. A considerable number of uncommitted connector pins are provided, making it possible to support a 16 bit processor if desired.

unmodified TV set. The latter is possible because the display signal has a bandwidth of slightly more than 6 MHz.

Construction of the TV Readout portion of this card requires considerable care due to the high density of the data paths. It took me about 5 hours to assemble this part of the board. Unfortunately, in my haste to see something on the screen I overlooked the soldering of an IC pin. When the system was first turned on, writing to the display buffer produced no change on the screen. I was lucky — impatience cost me only an hour of Sherlock Ohmsing — you may not be so fortunate. One last piece of advice; epoxy the crystal to the card to ruggedize your system.

Cassette interface

1100 bits per second is a fairly high data transfer rate for an inexpensive mass storage system. This is the primary feature of this cassette interface. Data is recorded by converting a logic one (called a Mark) to a 2125 Hz. tone and a logic zero (Space) to a 2975 Hz. tone. This is accomplished with an extraordinarily simple 566 voltage controlled oscillator (VCO) circuit.

The frequencies chosen for use with this frequency shift recording technique are widely spaced and are unrelated harmonically, providing good signal/noise ratio recording with any reasonably stable cassette recorder. Bit 0 of port No. 1 is used to input the data to be recorded. Memorex MRX2 or Maxell UD tape is recommended for optimum reliability. In addition, the DG recommends not using the first minute or so of any commercially prepared tape as their experience indicates a statistically high drop-out rate in this area of the tape due to handling.

data recovery

Audio tone-to-digital data conversion is performed by several op amp stages. The raw recorded output is clipped, passed by one of two active bandpass filters to a full wave detector, low-pass filtered to remove any remaining audio component, and adjusted to the proper TTL level for input to the processor.

The open layout of the cassette interface portion of this card reduces the risk of solder shorts. The lack of silk screened component labels on the card, however, makes it slow going

(component designations are specified in the assembly documentation).

Alignment and construction of the cassette section required about three hours to complete. Accurate alignment is required for optimum reliability, especially at a rate as high as 1100 bits/second.

The VCO circuit requires two simple adjustments; set the Mark potentiometer to 2125 Hz. with a logic one applied to the interface input; then apply a logic zero and adjust the Space potentiometer for 2975 Hz. at the output. A final tune-up is performed by programming the computer to supply the logic levels to the interface input and again trimming the Mark and Space potentiometers. The cassette interface is now ready to record data.

Alignment of the data recovery section of the cassette interface requires three simple adjustments. A scope and a source of clean audio signals (2125 Hz. and 2975 Hz.) will be needed. The two active filters are peaked at their desired bandpass frequencies by paralleling trimming resistors on the filters. The final adjustment involves setting the Read Offset potentiometer for a Mark Hold condition when no tone is applied to the interface input. The Cassette interface is now ready for use. If you wish, the DG will make the final alignment for \$20.00. If a 'fix-it' is also required (sorry — basket cases will not be accepted), send \$30 when returning the card.

8K Memory Card

If you've seen one 8K RAM card, you've seen them all. While I am quite impressed with the practical design approach which the DG has employed throughout their products, I was a little disappointed with their ultra-

plain 8K Memory card. There is no convenient DIP switch to select the address decoding (the board can be strapped to reside in one of 8 blocks of memory; 0-8K, 8K-16K, etc.). My main objection, however, is that there is no voltage regulator on this board. One voltage surge on the power line and it's 'Goodbye Mr. Chips.' I wish someone would pass a law to make it mandatory to put voltage regulators on memory boards and CPU cards. 2102-1's are standard with this card. That means that each 8K board will draw nearly 2 Amps.

Since there are 64 1K X 1 memory chips, they are wired up to produce an 8K X 8 matrix. The address lines are buffered with 7404's. There is a section of a 7420 four input NAND gate used to degate the RAM, permitting use of valuable lower address space by both RAM and ROM.

I would recommend that you construct this board in two settings; do one side of the board, move onto another board, then return and finish the 8K RAM board. This will help you avoid fatigue caused by the never-ending task of soldering row-upon-row of DIP pins. Without this break it is very easy to overlook a pin to be soldered or worse still, a fatal bridge. If you do make an error on this board, the DG group has concocted a super nifty memory test program to pinpoint the trouble, as we shall see.

Z-80 CPU card

EPROM bootstrap loading on this board provides you with 'power-on smarts' to eliminate the need for toggling in this information from a front panel. DMA circuitry makes it possible for you to add a front panel in case of emergency debugging requirements. 2K of address strappable RAM is provided on

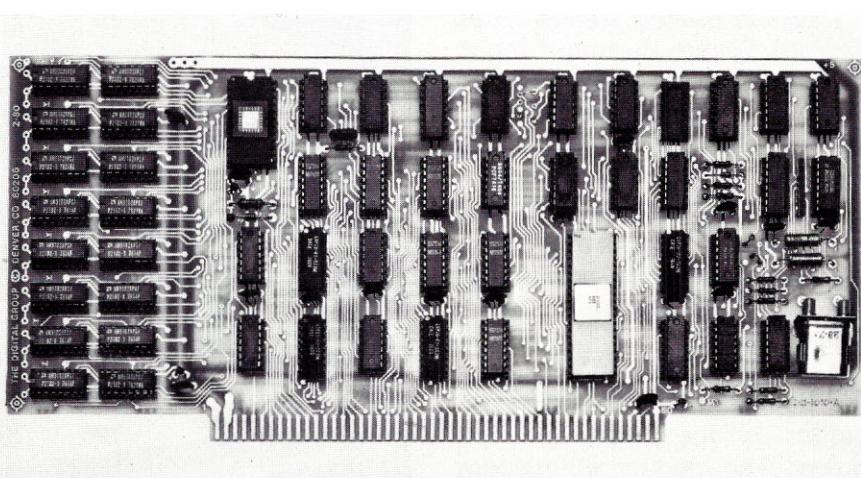


photo 6. The EPROM bootstrap loader and the 2K of RAM are on the left side of this Z-80 CPU board. Great care must be used in assembling this card due to the close proximity of the conductors. The external interrupt socket is the empty one near the top of the board on the right.

this card to store the operating system which we will discuss shortly.

This is a good place to mention one of the characteristic features of the DG system; processor independent system design. If you are concerned about newer and better microprocessor chips appearing on the market and what effect this will have on your investment, the DG system is for you. DG has an ongoing program of offering the latest and most popular processor chips designed onto cards which can be used to directly replace your present DG CPU. In fact, they have offered an 8080-to-Z-80 upgrading kit so you could strip the expensive parts from your 8080 board, buy the upgrade kit containing the Z-80 and other parts, put it together and presto — your mild mannered 8080 board has turned into the powerful Z-80 board, able to leap tall instructions in a single bound! As you can see, the DG is wise when it comes to spending your money.

Take your time constructing this board. It took me 9 hours of careful assembly and checking with a voltmeter for proper DIP socket voltages before I went for

the 'big switch' and the moment of truth. Data paths are dense as you can see from **photo 6**. My experience with computer kits has instilled in me a great respect for the care which *must* be exercised during the assembly of CPU boards such as this where the high density data paths seem to attract solder splashes and wayward strands of wire. Pretend that you are assembling the main board for a NASA Mars probe — it might help.

A calibrated scope is required to confirm that the clock is oscillating at exactly 2.5 MHz. Even a slight error here will be amplified many times by software timing loops. Program a time-of-day clock to check this frequency if you do not have access to a quality scope.

DG software support

The DG has a professional software group to generate programming support. Their major object, I would say, is user convenience. This systems approach is embodied in the Operating System Cassette which transforms the collection of hardware into a real 'computer.'

Cassette Read, Cassette Write, Storage Dump, Keyboard Input, and the Operations Monitor are the five programs which comprise the operating system. DG cautions the user to stay above location 006 000 (octal) unless you wish to overwrite the operating system (if you do, merely reload the Operating System Cassette).

After thoroughly DC checking the system and inspecting for solder bridges, turn on the power. The monitor will display, "READ Z-80 INITIALIZE CASSETTE." Load the operating system from a cassette recorder and observe the screen. If a ":" shows up instead of the octal page number of the data being read in, your system has determined that a bit of data has been read incorrectly. Reload and start again. I would recommend that you modify the remote speaker jack on your cassette recorder so that you can hear the data as it flows into the interface. This will permit you to locate the operating system beginning and end, as well as that of other programs on tape.

The user options will be displayed on the screen as shown in **photo 7**. The jump in the option numbers is due to a program improvement made by the DG software people. READ and WRITE are the cassette operating programs and are used as you might expect. Options 3 and 4 are the DUMP program, 3 providing an octal dump, 4 a hex dump. For example, select option 3 (via the keyboard) and the registers and flags of the Z-80 will instantly appear on the screen. Press the Space key to page through memory, 96 bytes at a time (it's just like flipping the pages of a book). This memory scanning feature makes it easy to locate unused memory for new programs.



photo 7. Although I did not buy this fancy monitor offered by the DG, this photo does show the clarity of the readout and the software options posed by the operating system.

BASIC, games, etc.

MAXI-BASIC is the high-level programming language offered by the DG. It contains all the features of standard BASIC and then some. This version of BASIC occupies 8K and the DG recommends that you have at least 18K to run it. MAXI-BASIC is available on a cassette from the DG for \$15.

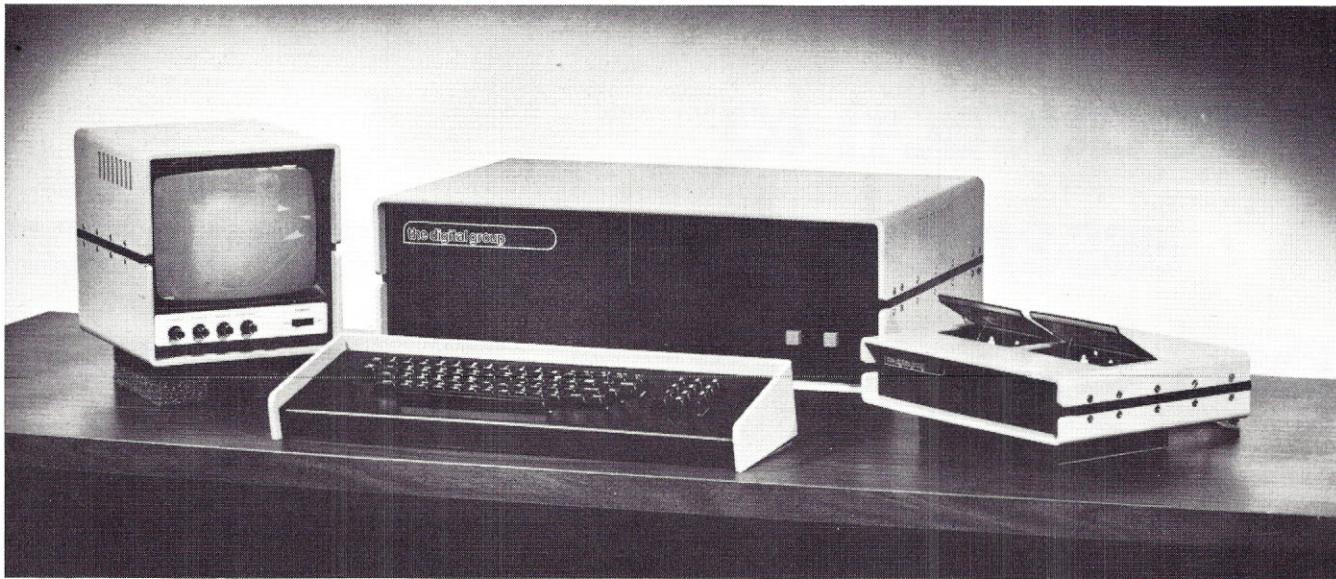
And speaking of BASIC, Tiny BASIC Extended (TBX-Z80) is offered for \$5, also on a cassette. Why, you ask, should you buy an abbreviated version of BASIC when you can get MAXI-BASIC to feed your Z-80? Well, the DG collection of games on cassettes must run under TBX-Z80, that's why. So, if you're a gamesman (gamesperson?), be sure to get the TBX-Z80. The DG offers not just one, but six Tiny BASIC Game Cassettes. See the DG Flyer No. 8 for the full games listings. By the way, the CLOCK program on Set 3 has a problem — the timing loops were not completely adjusted to the Z-80 speed (the games were adapted from their 8080 versions) — don't set your watch by the CLOCK. For Z-80 ignoramuses, there is the Z-80 Educator

Cassette. This program will quickly teach you about the Z-80 instructions and addressing modes.

Back to the Operating System Cassette, we find six neat little routines on the tape after the operating system. There is the CW KEYBOARD routine — outputs keying signals for a code generator on the LSB of port 2. It has a software FIFO which permits the operator to get up to 256 characters ahead of the character being sent. The RTTY-TO-ASCII routine converts FSK at 60 wpm (Baudot) to ASCII. BRAIN TEASER is a game for stretching your gray matter. Use FREQUENCY COUNTER to align your cassette interface, if need be. STAR SPANGLED BANNER was the routine mentioned at the beginning of this article. Finally, we get to MEMORY TESTER. Use this program to check out your 8K RAM boards. It prints out (are you ready) the IC number of any memory chip which it finds to be faulty. Not only that, but this program automatically 'knows' how much memory you have in your system. Now that's convenience.

conclusion

The Digital Group offers a very complete, conservatively designed system. The quality of the hardware, I have found, is excellent. Perhaps the most outstanding features are the processor independent system design to cope with advances in the technology (or applications requirements) and the user convenience of their software. From their delivery, sales, and repair policies, I find that they are reliable and responsive, and that's important. If that's what you're looking for (and you should be), then perhaps it's time to give the DG a call and request their complete flyer package to see if you agree with my assessments. **END**



Cabinets clockwise from top: CPU, Dual-cassette drive, Keyboard, 9" Monitor.

Meet The Digital Group

If you are seriously considering the purchase of a microcomputer system for personal or business use...or just beginning to feel the first twinges of interest in a fascinating hobby...the Digital Group is a company you should get acquainted with.

For many months now, we've been feverishly (and rather quietly) at work on our unique, high-quality product—a microcomputer system designed from the inside out to be the most comprehensive, easy-to-use and adaptable system you'll find anywhere. And our reputation has been getting around fast. In fact, you may have already heard a little something about us from a friend. We've found our own best salesmen are our many satisfied customers.

There's a good reason. Simply, the Digital Group has a lot to offer: state-of-the-art designs, a totally complete systems philosophy, unexcelled quality, reasonable software, affordable prices and the promise that our products will not become rapidly obsolete, even in this fast-moving, high-technology field.

The Advantages

Here are a few specific advantages of our product line:

- We offer interchangeable CPUs from different manufacturers (including the new "super chip"—the Z-80 from Zilog) which are interchangeable at the CPU card level. That way, your system won't become instantly obsolete with each new design breakthrough. The major portion of your investment in memory and I/O is protected.
- Digital Group systems are complete and fully featured, so there's no need to purchase bits and pieces from different manufacturers. We have everything you need, but almost any other equipment can be easily supported, too, thanks to the universal nature of our systems.
- Our systems are specifically designed to be easy to use. With our combination of TV, keyboard, and cassette recorder, you have a system that is quick, quiet, and inexpensive. To get going merely power on, load cassette and go!
- Design shortcuts have been avoided—all CPUs run at full maximum rated speed.
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introduction to assembly language translation

part two

by Michael Wimble
6026 Underwood Ave., S.W.
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In the first part of this short course on assembly language translation we discussed the organization and general features of a three-pass assembly language translator. Continuing with the discussion, this article examines phase one of the translator. Topics include: statement scanning, label processing, intermediate text generation, building and organizing a symbol table, and op code and operand processing. The translator considered here was written for the IBM System III computer. This assembler provides a wide range of user options. We will consider restrictions imposed to match this translator to systems which have a major resource limitation, such as a small main memory in the typical microcomputer.

phase one overview

As stated in part one of this series, the translator converts source programs (computer instructions written by the programmer) into strings of numbers which have precise meanings and are convenient to manipulate during the translation process. These strings of numbers are called *intermediate text*. An overview of the process

used to generate intermediate text is shown in **fig. 1**. As shown in this flowchart, phase one of the translator performs the following for each source statement encountered in the program: the label attached to the statement is processed (just how this is done will be covered later) if any label is present; the op code (operation code) is extracted (this process will also be considered later), and for each particular op code there is a unique subroutine which is called to process the remainder of the source statement. The intermediate text produced during this phase must accurately express both the syntax (statement structure) and the semantics (precise meaning) of the source statements. In addition, intermediate text must contain several items of information describing the relationship of each source statement to the rest of the program.

Keeping this simple view of phase one in mind, we now turn to consider the content and format of the intermediate text to be generated by phase one. Later, the basic elements of information, called *tokens*, which are used to generate the intermediate text will be dis-

cussed. The examination of phase one of an assembly language translator will conclude with a discussion of the subroutines and tables which comprise an important part of the translation process.

intermediate text

Each source statement is scanned by a subroutine which is appropriately called SCAN. This routine recognizes and extracts the semantic elements (the identifiable units of information) encountered in each source statement. The extracted semantic elements are then converted into intermediate text (number strings) containing the following information:

1. The statement number
2. The statement label (if present)
3. The value of the location counter when the statement was found
4. The op code
5. The length (in bytes) of the code to be generated by the translation
6. The operand expression in postfix notation (as discussed in Part One)
7. A description of the format of the operand
8. Error information

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fig. 1. General flow of phase one showing the relationship of major subroutines.

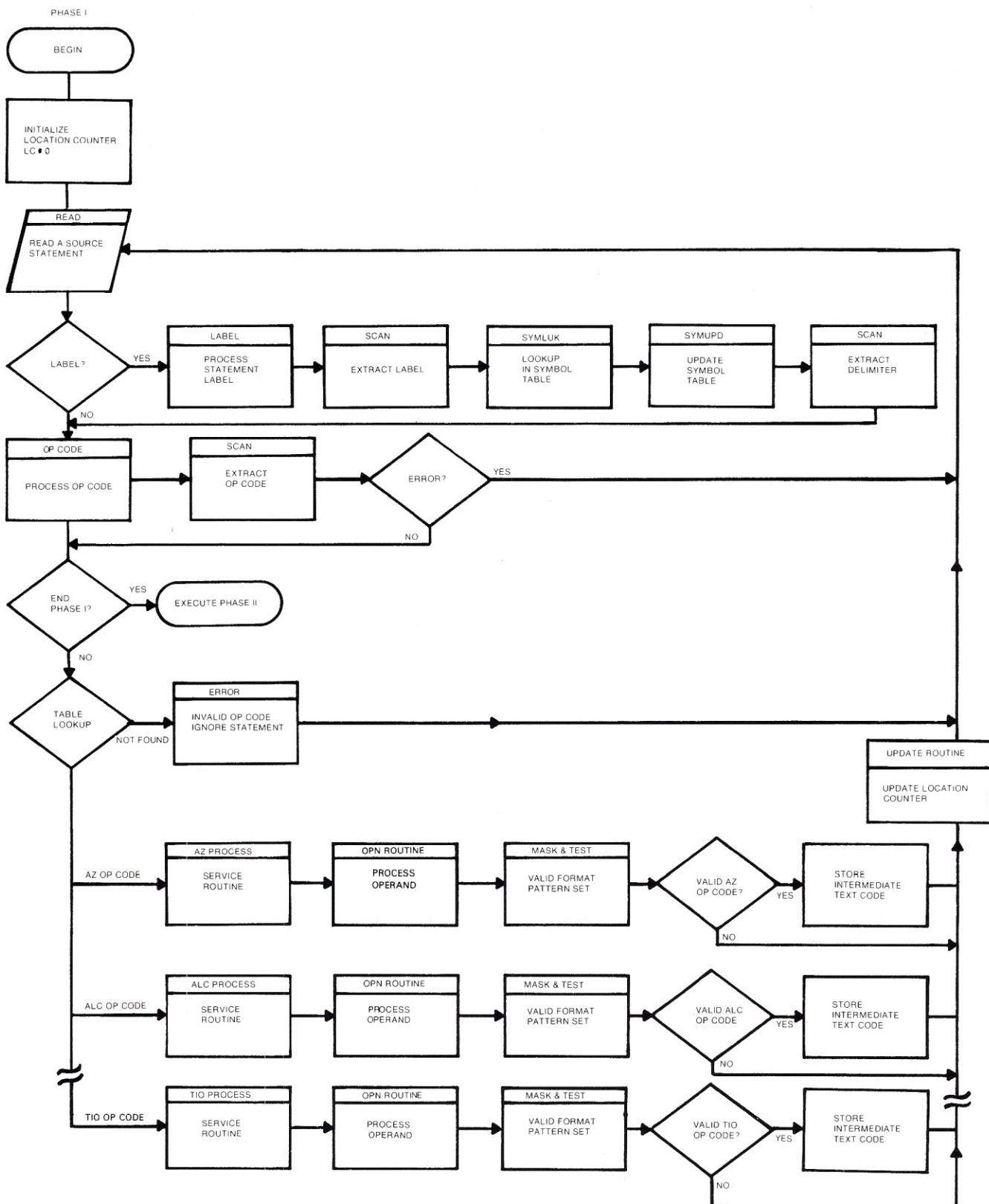


table 1. Program verbs are encoded using this Hex chart. Below are the definitions of these verbs.

VFRB HEX CODING TABLE

| 1ST HEX DIGIT | 0 | 1 | 2 | 3 | 8 |
|---------------|-------|--------|-------|---------|--------|
| 2ND HEX DIGIT | | | | | |
| 0 | FILL | SPACE | YABS | IF | *CSECT |
| 1 | LTRM | EFFECT | XABS | THEN | *ASECT |
| 2 | ORG | TITLE | REC# | ELSE | *USECT |
| 3 | DROP | EQU | PRPA | #ARG | *DATA |
| 4 | USING | LOC | PLPA | *LENGTH | *DO |
| 5 | TEXT | MASK | *TLS | ABS | *ELSE2 |
| 6 | TFXT | LABEL | SFT | *NARG | *FIN |
| 7 | DBS | OB | MOD | *CCM | *DOL |
| 8 | DBC | ALEN | NEQ | *NCM | *GEN |
| 9 | DS | ALOC | LE | NUMBER | 01 |
| A | DC | ERR | GE | ELPA | D2 |
| B | END | OPND | XOR | UNEG | L1 |
| C | EXTRN | ACOD | UNDEF | *SLPA | L2 |
| D | ENTRY | RCOD | SYM | ARGS | X1 |
| E | START | FABS | *TEST | RTRM | X2 |
| F | PRINT | ZABS | *CNT | *SRPA | *CERR |

* => UNIMPLEMENTED EXTENSIONS

MNEMONIC DEFINITION

| | |
|--------|--|
| FILL | FILL CHARACTER. USED TO PAD TEXT IF NECESSARY, IGNRED. |
| LTRM | LEFT TERMINATOR. FIRST BYTE OF TEXT, SIGNALS BEGINNING. |
| ORG | ORIGIN DIRECTIVE SCANNED. |
| DROP | DROP BASE REGISTER DIRECTIVE SCANNED. |
| USING | USING BASE REGISTER DIRECTIVE SCANNED. |
| TEXT | TFXT OP CODE SCANNED. OPERAND FIELD WILL CONTAIN A TEXT STRING. |
| TFXT | TFXT OP CODE SCANNED. OPERAND FIELD WILL CONTAIN A TEXT STRING. |
| DBS | DEFINE STORAGE. LABEL ASSIGNED LOCATION OF 1ST BYTE RESERVED. |
| DBC | DEFINE CONSTANT. LABEL ASSIGNED LOCATION OF 1ST BYTE RESERVED. |
| DS | DEFINE STORAGE. LABEL ASSIGNED LOCATION OF LAST BYTE RESERVED. |
| DC | DEFINE CONSTANT. LABFL ASSIGNED LOCATION OF LAST BYTE RESERVED. |
| END | END DIRECTIVE SCANNED. |
| EXTRN | EXTRN DIRECTIVE SCANNED. |
| ENTRY | ENTRY DIRECTIVE SCANNED. |
| START | START DIRECTIVE SCANNED. |
| PRINT | PRINT DIRECTIVE SCANNED. |
| SPACE | SPACE DIRECTIVE SCANNED. |
| EFFECT | EFFECT DIRECTIVE SCANNED. |
| TITLE | TITLE DIRECTIVE SCANNED. |
| EQU | EQU DIRECTIVE SCANNED. |
| LOC | LOCATION COUNTER REFERENCE IN EXPRESSION. |
| MASK | MASK_FOLLOWS IN NEXT TWO BYTES. THE MASK CONTAINS SWITCHES INDICATING WHICH OF THE POSSIBLE PARTS OF AN OPERAND ARE ENCOUNTERED. FOR THIS TRANSLATOR AN OPRAND CAN OCCUR IN THE FOLLOWING FORMAT: D1(L1,X1),D2(L2,X2) AND EACH BIT IN MASK DENOTES ONE OF THE POSSIBLE ELEMENTS OF THE FORMAT FOUND. |
| LABEL | SYMBOL NUMBER OF LABEL FOR THIS STATEMENT FOLLOWS IN NEXT TWO BYTES. |
| DS | Q-BYTE OF INSTRUCTION FOLLOWS IN NEXT BYTE. |
| ALFN | LENGTH OF ASSEMBLED CODE FOR THIS STATEMENT FOLLOWS IN NEXT TWO BYTES. |
| ALOC | VALUE OF LOCATION COUNTER FOR STATEMENT FOLLOWS IN NEXT TWO BYTES. |
| FRR | ERROR DEFINITION FOLLOWS IN NEXT TWO BYTES. 1ST BYTE IS COLUMN NUMBER, SCANNED WHEN ERROR OCCURRED, 2ND BYTE IS ERROR NUMBER. |
| OPND | OPERAND EXPRESSION FOLLOWS. 1ST BYTE FOLLOWING IS LENGTH OF OPERAND. EXPRESSION STRING FOLLOWS. |
| ACOD | ABSOLUTE DATA FOLLOWS. 1ST BYTE IS LENGTH OF DATA STRING. DATA STRING FOLLOWS. |
| RCOD | RELOCATABLE DATA FOLLOWS. 1ST BYTE IS LENGTH OF DATA STRING. DATA STRING FOLLOWS. |
| FABS | FORMAT 'F' OP CODE FOLLOWS IN NEXT BYTE. |
| ZABS | FORMAT 'Z' OP CODE FOLLOWS IN NEXT BYTE. |
| YABS | FORMAT 'Y' OP CODE FOLLOWS IN NEXT BYTE. |
| XABS | FORMAT 'X' OP CODE FOLLOWS IN NEXT BYTE. |
| REC# | STATEMENT NUMBER FOLLOWS IN NEXT TWO BYTES. |
| PRPA | RIGHT PARENTHESIS FOLLOWING X1 OR X2 SCANNED. |
| PLPA | LEFT PARENTHESIS PRECEEDING L1 OR L2 SCANNED. |
| TLS | UNDEFINED. |
| SFT | SHIFT OPERATOR SCANNED. ('**') |
| MOD | MODULUS DIVIDE OPERATOR SCANNED. ('//') |
| NEQ | NOT EQUAL OPERATOR SCANNED. ('!=') |
| LE | LESS THAN OR EQUAL OPERATOR SCANNED. ('<=') |
| GE | GREATER THAN OR EQUAL OPERATOR SCANNED. ('>=') |
| XOR | EXCLUSIVE OR OPERATOR SCANNED. (' ') |
| UNDEF | UNDEFINED SYMBOL ENCOUNTERED. |
| SYM | SYMBOL # OF SYMBOL IN EXPRESSION FOLLOWS IN NEXT TWO BYTES. |
| TEST | UNDEFINED. |
| CNT | UNDEFINED. |
| IF | IF OPERATOR SCANNED. ('F') |
| THEN | THEN OPERATOR SCANNED. ('"N") |
| ELSE | ELSE OPERATOR SCANNED. ('"E") |
| ARG | UNDEFINED. |
| LENGTH | UNDEFINED. |
| ABS | ABSOLUTE VALUE OPERATOR SCANNED. ('"A") |
| NARG | UNDEFINED. |
| COM | UNDEFINED. |
| NCOM | UNDEFINED. |
| NUMBER | ABSOLUTE NUMBER IN EXPRESSION FOLLOWS IN NEXT TWO BYTES. |
| ELPA | EXPRESSION LEFT PARENTHESIS. (APPEARS ONLY IN STACK) |
| UNFG | UNARY NEGATIVE OPERATOR SCANNED. ('-') |
| SLPA | UNDEFINED. |
| ARGS | ARGUMENT SEPARATING COMMA SCANNED. |
| RTRM | RIGHT TERMINATOR. MARKS END OF INTERMEDIATE TEXT |
| D1 | D1 EXPRESSION FOLLOWS IN NEXT 3 BYTES. 1ST BYTE IS ZERO FOR ABSOLUTE EXPRESSION. NON ZERO FOR RELOCATABLE. BYTES 2-3 ARE VALUE. |
| D2 | D2 EXPRESSION FOLLOWS IN NEXT 3 BYTES. 1ST BYTE IS ZERO FOR ABSOLUTE EXPRESSION. NON ZERO FOR RELOCATABLE. BYTES 2-3 ARE VALUE. |
| L1 | L1 EXPRESSION FOLLOWS IN NEXT 3 BYTES. 1ST BYTE IS ZERO FOR ABSOLUTE EXPRESSION. NON ZERO FOR RELOCATABLE. BYTES 2-3 ARE VALUE. |
| L2 | L2 EXPRESSION FOLLOWS IN NEXT 3 BYTES. 1ST BYTE IS ZERO FOR ABSOLUTE EXPRESSION. NON ZERO FOR RELOCATABLE. BYTES 2-3 ARE VALUE. |
| X1 | X1 EXPRESSION FOLLOWS IN NEXT 3 BYTES. 1ST BYTE IS ZERO FOR ABSOLUTE EXPRESSION. NON ZERO FOR RELOCATABLE. BYTES 2-3 ARE VALUE. |
| X2 | X2 EXPRESSION FOLLOWS IN NEXT 3 BYTES. 1ST BYTE IS ZERO FOR ABSOLUTE EXPRESSION. NON ZERO FOR RELOCATABLE. BYTES 2-3 ARE VALUE. |
| CERR | UNDEFINED. |

Table 1 shows the Hex coding plan used to translate program verbs into intermediate text. **Fig. 2** provides an example which demonstrates the format and content of the intermediate text produced for two statements encountered in a source program. The 'X, Y, Z' formats specify the arrangement of elements used to form the op code.

It should be clear that intermediate text is produced by scanning the source statement, extracting the semantic elements one by one, converting them into internally useable number strings, reordering these numbers, and adding descriptive information such as statement numbers and location counter values. The next section describes the subroutine responsible for scanning the source statement, extracting the semantic elements, and partially converting these into intermediate text.

SCAN-token extraction

A token is the basic unit of semantic information in any programming language statement. Any combination of characters may constitute a token, while combinations of tokens constitute a statement, and combinations of statements constitute a program. The bulk of programming language translation consists of manipulating tokens. As a result, a subroutine called SCAN has been developed to extract tokens from source statements.

As each source statement is read, pointers are initialized so that SCAN begins searching at the first character of the record. Each call to SCAN (i.e., "CALL SCAN") results in the extraction of the next semantic unit of information. This extracted element is stored in a buffer memory and flag bits are set to describe what has been found

by SCAN. This descriptive information is *returned* to the calling program to aid in the translation process.

tokens

Tokens fall into one of two broadly defined classes: identifiers and operators. Operators are, of course, symbolic mathematical operators (+, /, etc.). Operators also include delimiters (blanks, (), etc.). Identifiers are then tokens which are not operators. Identifiers consist of symbols (A, 16XZM, etc.) and numbers (-1, 36287, etc.). A token is *terminated* by the occurrence of an operator. **Table 2** shows the single character operators for the sample translator.

To illustrate the operation of subroutine SCAN, **fig. 3** shows the flowchart for SCAN and **tables 3 and 4** list the communication variables and bit switches used by SCAN. **Fig. 4** illustrates the operation of SCAN as tokens are extracted from a sample source statement.

communication bits

As shown in **table 4**, there are 8 communication bits which can be set by SCAN to describe the token which it has found. The calling routine must test for the various conditions indicated by these communication bits on return from SCAN. If SYMF (SYMBOL Found) is set, then either a symbol or a number was scanned; if both ALFA ("ALFAbetic") and SPEC (SPECial) are reset, a number was scanned; otherwise a symbol was scanned. If a number was found, the first three bytes of SCTOK (SCan TOKen) contain the 24 bit representation of the number. A scanned symbol is stored left justified in the correct character format beginning at SCTOK.

If LITS (LITERAL Scan) is set a literal was scanned. The literal is stored in character format, left

fig. 2. Example of intermediate text generated for two typical source statements.

| <u>STMT</u> | <u>LABEL</u> | <u>STATEMENT</u> |
|-------------------|--|----------------------------|
| 50 | LOOP1 | AZ SUM(5),HOURS(3*LEN,XRL) |
| 51 | | LA 1(,XRL),XRL |
| <u>TEXT (HEX)</u> | <u>MEANING</u> | |
| 22 00 32 | Statement No. 50 | |
| 2D 00 11 | Label is symbol No. 17 (LOOP1) | |
| 19 04 0C | Location counter value is 040C (HEX) | |
| 21 06 | The 'X format' op code is 06 (AZ) | |
| 18 00 05 | Length of code to be generated is 5 bytes | |
| 15 E7 F8 | Standard operand form is: D1(L1),D2(L2,X2) | |
| 1B 15 | Operand expression is contained in the next 21 bytes | |
| 2D 00 12 | Symbol is No. 18 (SUM) | |
| 24 | Left parenthesis: (| |
| 39 00 05 | The number 5 | |
| 23 |) | |
| 3D | , argument separator | |
| 2D 00 31 | Symbol No. 49 (HOURS) | |
| 24 | (| |
| 39 00 03 | The number 3 | |
| 2D 00 13 | Symbol No. 19 (LEN) | |
| 5C | * (an EBCDIC character) | |
| 6B | , (" ") | |
| 2D 00 14 | Symbol is No. 20 (XRL) | |
| 22 00 33 | New statement No. is 51 | |
| 19 04 11 | Location counter value is 0411 (HEX) | |
| 1F 02 | The 'Z format' op code is 02 (LA) | |
| 18 00 03 | Length of code to be generated is 3 bytes | |
| 15 9F 00 | Standard operand form is: D1(,X1),D2 | |
| 18 0D | Operand expression follows in the next 13 bytes | |
| 39 00 01 | The number 1 | |
| 24 | (| |
| 3D | , argument separator | |
| 2D 00 14 | Symbol No. 20 (XRL) | |
| 23 |) | |
| 6B | , (an EBCDIC character) | |
| 2D 00 14 | Symbol No. 20 (XRL) | |

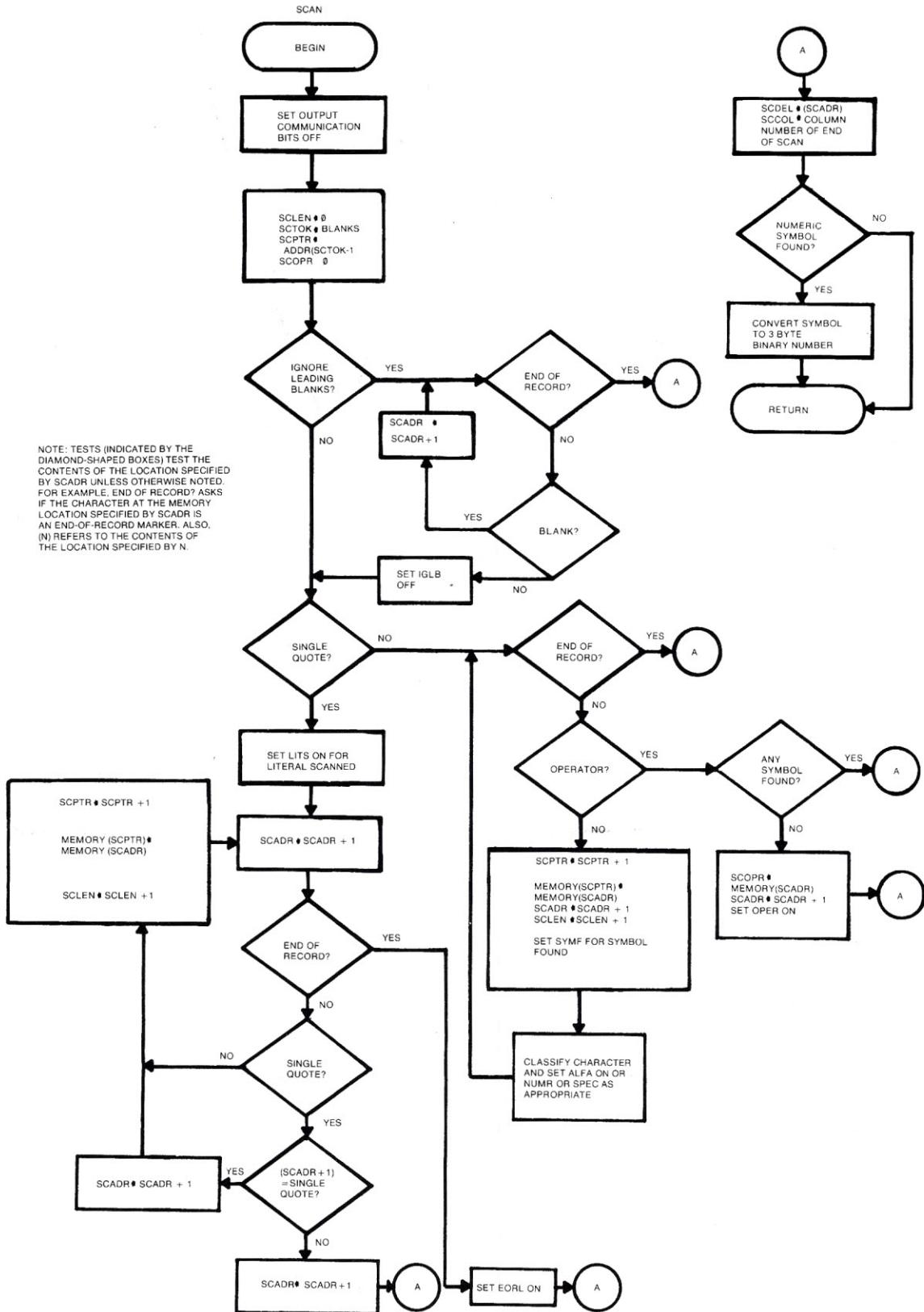


fig. 3. Flowchart of subroutine SCAN.

justified, beginning at SCTOK. When LITS is set, the assembler must test EORL (End Of Record Literal). EORL set means the closing quote for a literal was not found by the time the end of record was reached.

If neither LITS nor SYMF is set, one of two conditions has occurred: either an operator was scanned or the end of record was found. If an operator was scanned, OPER (OPERator) will be set.

| LABEL | STATEMENT | | |
|-------|-----------|-----------|----------|
| CALL | TOKEN | DELIMITER | OPERATOR |
| 1 | LOOP1 | blank | |
| 2 | AZ | blank | |
| 3 | SUM | (| |
| 4 | 5 | (| |
| 5 | 5 |) | |
| 6 | , |) | |
| 7 | H | , | |
| 8 | HOURS | (| |
| 9 | 3 | (| |
| 10 | * | * | |
| 11 | L | * | |
| 12 | LEN | , | |
| 13 | X | , | |
| 14 | XRL |) | |
| 15 | blank |) | |

fig. 4. Example of token extraction by subroutine SCAN.

IGLB switch

Before calling SCAN, the calling routine can set a bit called IGLB (IGnore Leading Blank). This condition causes SCAN to ignore leading blanks in any statement which it scans. The IGLB option is useful when trying to locate the beginning of the op code or operand fields. For instance, after having found the blank character which terminates the label field, the next call to SCAN should have set IGLB so that any blanks between the label and the op code fields will be ignored. The symbol returned will then be just the desired op code. Without this facility, the calling program would have to make repeated

table 2. Single character operators used in the sample translator.

| CHARACTER NAME | FUNCTION |
|----------------|---|
| , | comma label/argument/operand separator |
| ' | single quote enclosing literals |
| + | plus binary sum/unary positive value |
| - | dash binary subtract/unary negative |
| ~ | not logical inverse |
| * | asterisk location counter/binary multiply |
| / | slash binary divide operator |
| (| left parenthesis expression grouping/sub-parameter |
|) | right parenthesis definition (index register) closure of left parenthesis |
| < | less than relational binary operator |
| > | greater than relational binary operator |
| = | equal relational binary operator |
| | vertical bar logical binary operator OR |
| & | ampersand logical binary operator AND |

table 3. Communication variables used by subroutine SCAN.

| VARIABLE | NAME | FUNCTION |
|----------|--|----------|
| SCADR | Holds memory address of next character to be scanned | |
| SCCOL | Holds column number of end of scan (one column before delimiter) | |
| SCDEL | Holds delimiter encountered | |
| SCLEN | Holds length of symbol, number, or literal in SCTOK | |
| SCOPR | Holds operator scanned | |
| SCPTR | Holds memory address of last character put into SCTOK | |
| SCTOK | Holds extracted symbol, number, or literal | |

table 4. Communication bits (also called **switches**) used by SCAN.

| BIT | INPUT/ NAME | OUTPUT | FUNCTION |
|------|----------------|--------|---|
| IGLB | 0 | INPUT | ON means ignore leading blanks |
| LITS | 1 | OUTPUT | ON means literal was scanned |
| SYMF | 2 | OUTPUT | ON means symbol was scanned |
| ALFA | 3 | OUTPUT | ON means alphabetic character was scanned |
| NUMR | 4 | OUTPUT | ON means numeric character was scanned |
| SPEC | 5 | OUTPUT | ON means special character was scanned |
| OPER | 6 | OUTPUT | ON means an operator was scanned |
| EORL | 7 | OUTPUT | ON means end of record was found while scanning a literal |

calls to SCAN and examine the communication variables to determine when a symbol was finally found.

Having now defined a token, described its extraction and shown its ultimate use, we may continue with the discussion of the translator itself. The next section will detail label processing. Following this there will be a brief digression to discuss symbol tables before returning to the translation process.

LABEL subroutine

Fig. 5 shows the flowchart for subroutine LABEL. There is a feature implied here which is not found in many assemblers; the ability to assign multiple labels to a statement. This is useful for writing large programs, such as language translators, and does not cost much in terms of translator size or complexity. With the multiple label facility, several assignments can be accomplished with a single statement. For instance, to equate the three symbols "PARMREG", "R1", and "ONE" equal to a numerical value of 1 we can use a single statement:

PARMREG, R1, ONE EQU 1
instead of three statements as would be required by most other assemblers.

Following along **fig. 5**, the first step is to call SCAN (IGLB not set) to extract any symbol starting in column 1 of the record. If a literal or an operator is found, then error information is generated in the intermediate text string and the statement is ignored. If no symbol was found, a check is made for the blank character which terminates the label field. Absence of this blank indicates invalid statement syntax.

Having extracted the label, the next step is to call SYMLUK which performs two functions and is described in detail in the next section. First a check is

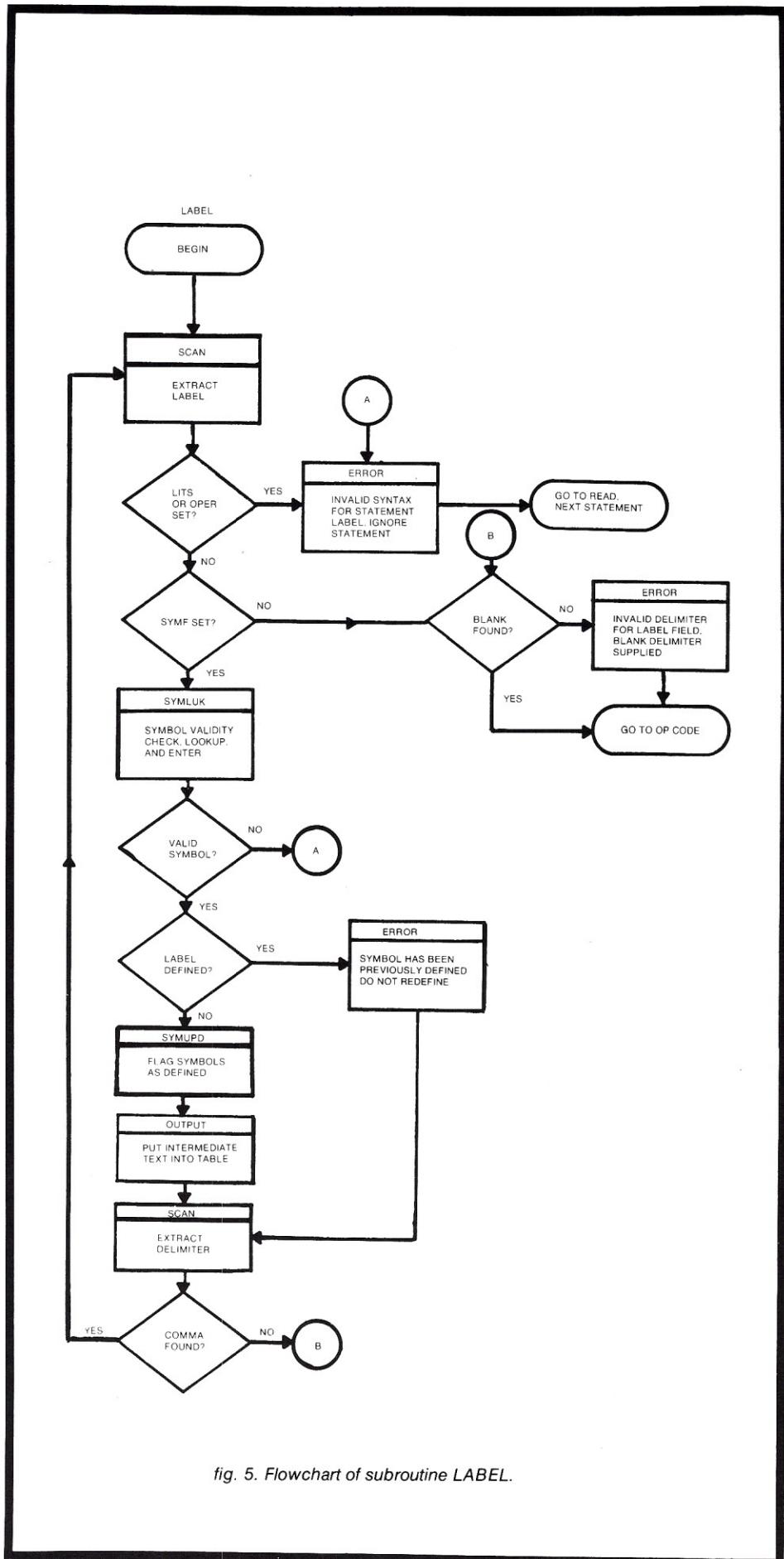


fig. 5. Flowchart of subroutine LABEL.

made to determine valid symbol syntax. If a valid symbol is found then a lookup is made in the symbol table to see if the symbol has already been entered. If the symbol is already in the table then it must have been previously found in an operand expression or as a label of a previous statement. A symbol appearing in a label field is said to be defined, so a symbol appearing as a label more than once would be multiply defined, which is an error. In either case, when a symbol is found in a label field its symbol table entry is updated to reflect that the symbol is defined. Symbols not already in the symbol table are added and flagged as defined.

After creating the intermediate text for any valid labels encountered, SCAN is invoked again to extract the label's delimiter. If a comma is found, the whole process is repeated, otherwise the previously described check for blank delimiter is performed.

Before proceeding with the description of the next step in the translation function, which is to extract and service the opcode, another digression will be made. The next section discusses the organization, content, and manipulation of the symbol table; important and necessary background material.

symbol table organization

The symbol table is perhaps the most important single element of a language translator. Symbolic manipulation is responsible for raising the level of programming from the tedium of machine language programming to the ease of high level language programming. Indeed, the power and popularity of a language is directly related to the facilities for symbol manipulation provided by the language.

In order to increase the utility of a symbol table, more information must be maintained, which

| BYTE | BIT | FUNCTION |
|---------|-----|--|
| 0 - 5 | | Character representation of the symbol |
| 6 - 7 | | Symbol value |
| 8 - 9 | | Statement No. where symbol is defined |
| 10 - 11 | | Implied length of symbol |
| 12 | | Other descriptive information as follows |
| | 0 | EXTRN symbol |
| | 1 | ENTRY symbol |
| | 2 | Multiply defined |
| | 3 | Value is resolved |
| | 4 | Value is absolute |
| | 5 | Symbol is name of module |
| | 6 | Macro switches in byte 15 apply |
| | 7 | Definition has been encountered |
| 13 - 14 | | Hash forward link (also XREF link) |
| 15 | | Macro processing switches |

fig. 6a. Byte definition of each of the 16 bytes of information required by the sample translator for every symbol table entry.

| BYTE | BIT | FUNCTION |
|-------|-----|--|
| 0 - 4 | | Character representation of the symbol |
| 5 - 6 | | Value of the symbol |
| | 7 | |
| | | Other descriptive information: |
| 7 | 0 | Multiply defined |
| | 1 | Value is resolved |
| | 2 | Value is absolute |
| | 3 | Definition has been found |
| | 4 | EXTRN or REF symbol |
| | 5 | ENTRY or DEF symbol |
| | 6 | Symbol is module name |
| | 7 | Available |

fig. 6b. Byte definition for a minimum size symbol table requiring only 8 bytes of information for each table entry.

table 5. Communication variables used by symbol table subroutines.

| VARIABLE | |
|----------|--|
| NAME | FUNCTION |
| SYEND | Number of symbols currently in table |
| SYMAX | Maximum number of symbols that can be stored in symbol table |
| SYNUM | Number of symbols found or to be updated |
| SYSYM | Copy of symbol found, to be created, or to be updated |

table 6. Communication bits used by symbol table subroutines.

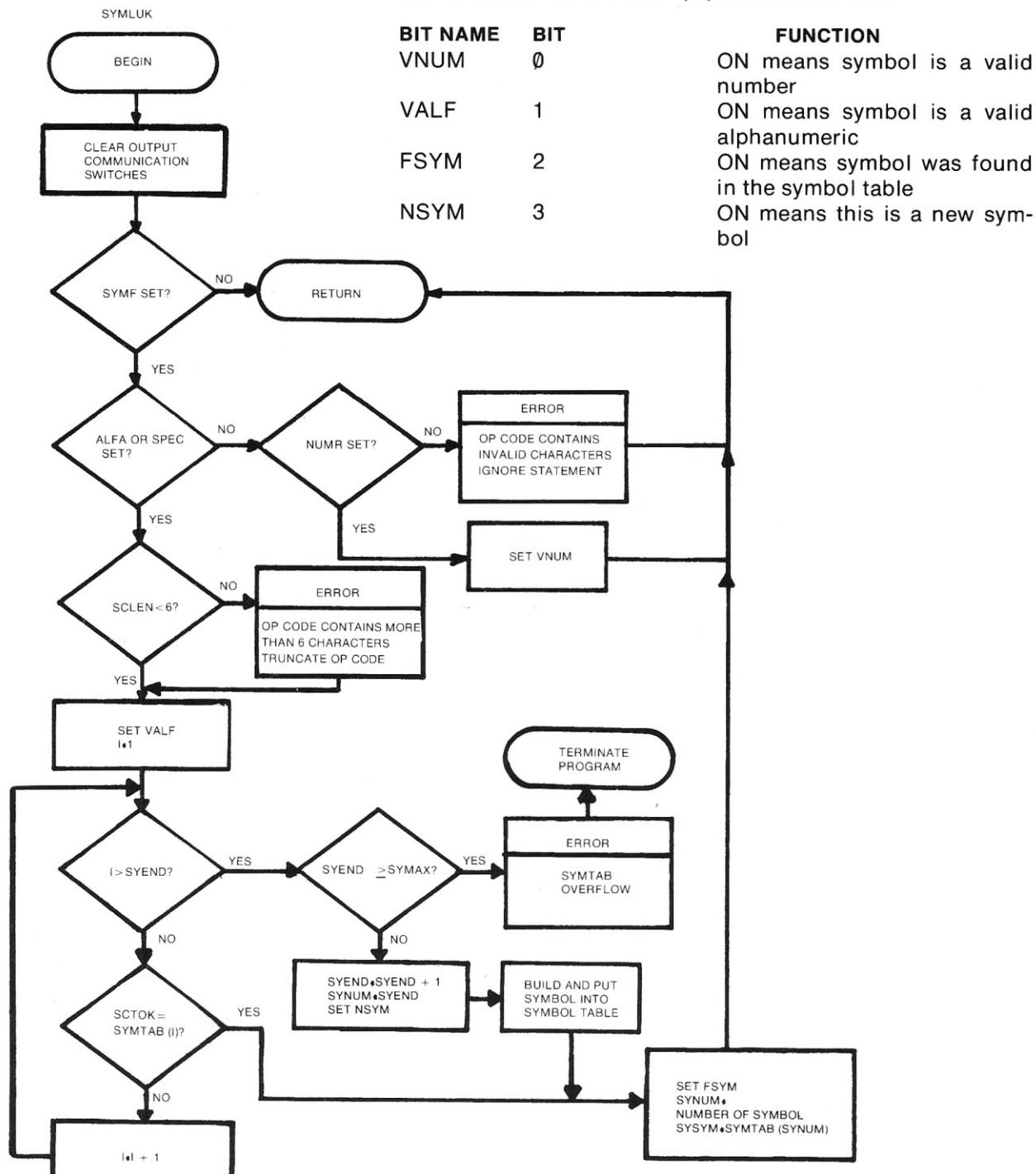


fig. 7. Flowchart of subroutine SYMLUK.

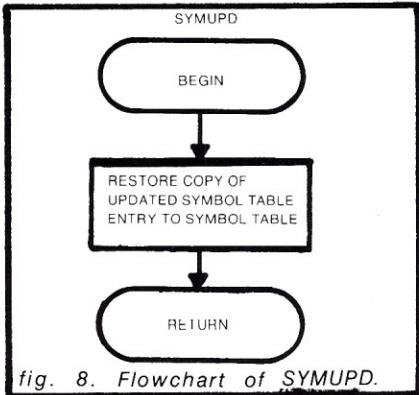


fig. 8. Flowchart of SYMUPD.

increases both the size and complexity of the table. This usually necessitates restricting the number of symbols that the translator can process in a single run. By reducing the amount of information maintained in the symbol table, more symbols may be processed at a cost of trading off many powerful features and conveniences, such as intelligent error recovery and macro processing.

As shown in **fig. 6a.**, each entry into the symbol table used by the sample translator requires 16 bytes of information. **Fig. 6b.** shows the minimum information needed by a useful translator.

The organization of a symbol table is at least as important as its content. The simplest organization is a *linear list* where new elements are added to the table immediately following the previous entries. To perform a symbol table lookup, that is to check if a symbol is already entered into the table, a comparison is made between the symbol to be found with each entry in the table until a match is determined or until the end of the table is reached. The single advantage of the linear list's simplicity must be weighed against the inordinate amount of time required to perform a lookup in this type of table.

In phase one of the translator, symbol table lookup is a very frequent activity. Storing a symbol table as a linear list instead of in a more sophisticated manner could mean the difference

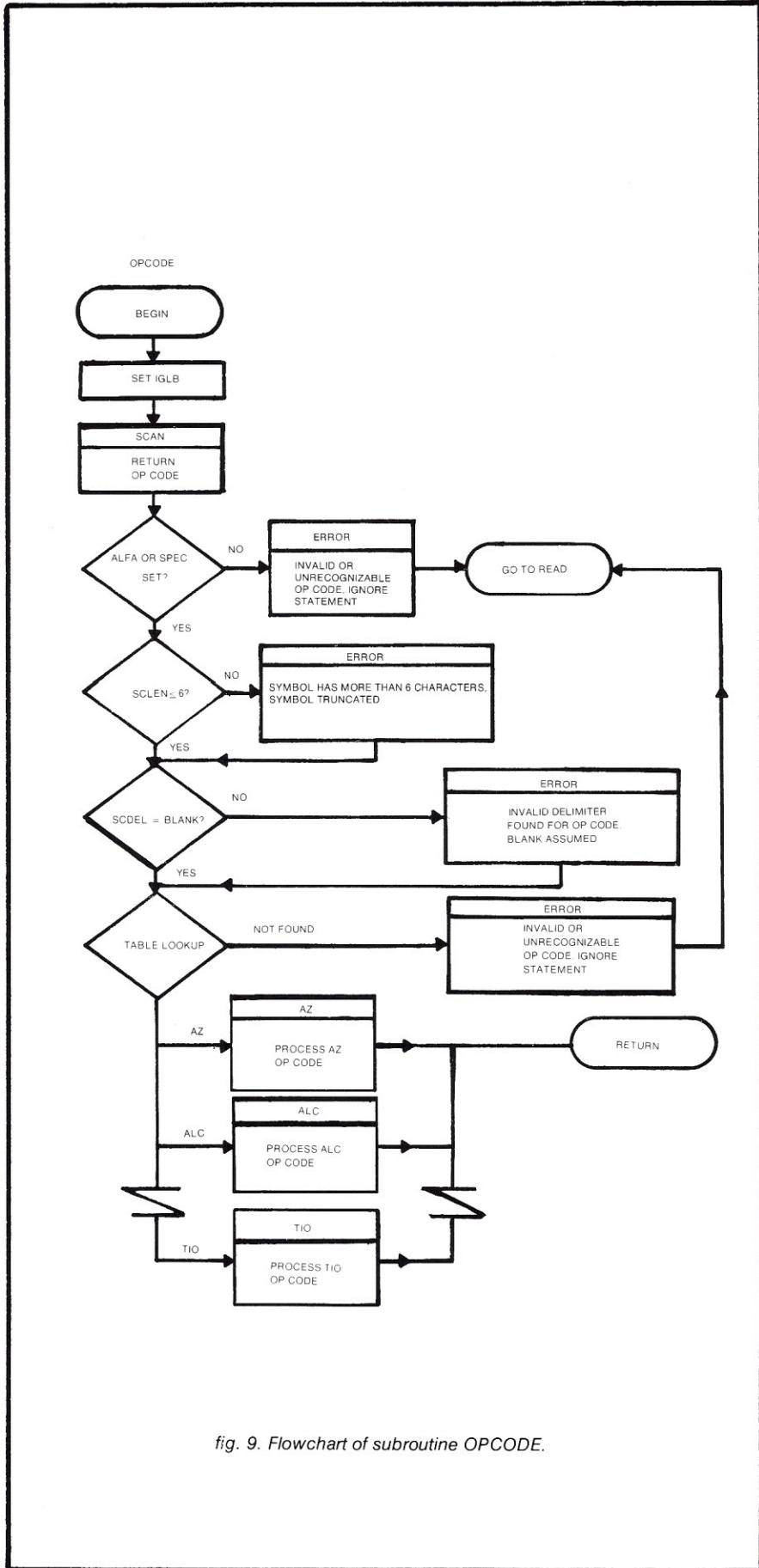


fig. 9. Flowchart of subroutine OPCODE.

| MASK BIT | MEANING OF BIT SET |
|----------|---|
| 0 | D1 found in operand |
| 1 | (after D1 found in operand |
| 2 | L1 found in operand |
| 3 | , between L1 and X1 found |
| 4 | X1 found in operand |
| 5 |) after X1 found in operand |
| 6 | , between operand subexpressions found in operand |
| 7 | D2 found in operand |
| 8 | (after D2 found in operand |
| 9 | L2 found in operand |
| A | , between L2 and X2 found |
| B | X2 found in operand |
| C |) after X2 found in operand |
| D | - not used - |
| E | - not used - |
| F | Operand could not be matched to valid pattern |

fig. 10. Definition of bits in the 16 bit mask (pattern) used to examine (compare) with encoded text to determine whether the text follows the proper format.

between a 30 minute translation versus a 30 second translation. For the purpose of illustration, the flowcharts in **fig. 7** and **fig. 8** assume that the symbol table is organized as a linear list. However, the table used in the sample translator employs hash coding, linked lists, and overflow tables to achieve highly efficient table searching and storage. This technique is not suitable for computers with small main memory.

SYMLUK and SYUPD

Phase one performs three operations on the symbol table: lookup, add, and update. Lookup and add are performed by the same subroutine, SYMLUK, while update is performed by SYMUPD.

Fig. 7 shows the logic involved in SYMLUK and **tables 5 and 6** list the appropriate communication variables and bits. It is convenient to let SYMLUK also perform some validation checks on the identifier, thus SYMLUK begins by checking the communication switches from SCAN. If SYMF is not set,

SYMLUK terminates since literals and operators are not a part of the symbol table.

If SYMF is set, meaning that an identifier of some sort was scanned, then ALFA and SPEC are checked. If one or both are set, then a valid symbol was found. Remember from Part One of this article that a valid symbol is any string of characters that can't be mistaken for something else. Well, if SYMF is set then the identifier scanned must be some combination of letters, digits, and special characters. If the identifier is composed solely of digits it must be a number, otherwise it is a valid symbol. Finding an identifier consisting solely of digits results in VNUM (Valid NUMber) being set while an identifier not containing any digits, alphabetic characters, or special characters is considered an error and error information is put into the intermediate text.

Having found a valid symbol, SYMLUK will only consider the first six characters significant, truncating longer symbols. VALF is set to indicate that the identifier is a valid symbol. Next, a

table lookup is performed to determine if the symbol is already in the table. If the symbol is not found it is added. Finally FSYM is set to indicate that the symbol was found and a copy of the table entry is saved in SYSYM for use by the calling routine.

Fig. 8 shows the simple process of symbol table update. The symbol table entry stored in SYSYM by SYMLUK is updated by the calling routine which eventually invokes SYMUPD to replace SYSYM into the symbol table.

We return now to describing the phase one translation process. The next section describes the extraction and processing of the op code. Following this we get into what can be called the "meat" of the assembler — the extraction and encoding of operand expressions.

OPCODE subroutine

Op code extraction and processing is relatively simple and is shown in **fig. 9**. A call is made to SCAN with a request to ignore leading blanks. The identifier returned is checked for validity: proper size, character set, and delimiter. A table lookup is then performed to determine if the op code is valid. If valid, the table also indicates the address of the subroutine which will complete the processing of the source statement.

Until now, the only intermediate text that has been created for a statement describes the statement number, the symbol numbers of any labels encountered, and error information for any errors which may have been detected. It remains for each service routine to complete the intermediate text for the statement. Depending upon the op code, the service routine must generate text to describe the value of the location counter, the number of bytes of machine code to be produced as a result

Reader Input

PLEASED WITH FLOWCHARTING

I was pleased when I received my first issue of MICROTREK in the mail. I was even more pleased when I saw what MICROTREK contained. I was particularly impressed by your article on flowcharting. It has helped me in writing programs a great deal. I am also in the market to buy a microcomputer. After reading your excellent article on the KIM-1 Microcomputer Module, I seriously started to consider the purchase of such a unit.

Matthew A. Treu
Student,
Milwaukee Technical High
School

PUBLIC SAFETY COMPUTERS

Although I am an electronics engineer, I have been involved in radio communications and therefore know little about computers. It is my hope, however, to correct this situation because of the tremendous impact computers are having upon public safety communications. Also, I would like to develop my own computer to work along with my interest (of some 35 years) in amateur radio. But, as I have indicated, I do not know enough at this time to ask a decent question in either hardware or software. So please have some very simple articles.

Erling R. Jacobsen, W9KBE
1438 34th Avenue
Rock Island, Illinois 61201

TERMINOLOGY BARRIERS

I hope that your publication continues to serve those without a background in computers. Most publications in this field assume that the reader is already in the field. Getting an understanding of the terminology used is a problem in itself.

Allan A. Simpson
17 Barberry Rd.
Winnipeg, Manitoba
Canada R2J 2G8

DON'T DROP OUT OF THE RACE!

Hope you guys have not decided to drop out of the micro-race. We have only just begun as they say. Down the road there is a new industry ahead. The reason I am saying this is that I haven't received a second issue on my subscription as yet and fear your demise.

Having once been a publisher of a small publication as well as the chief writer of it [*Have I got a job for you — Ed.*], I can readily appreciate the problems of starting up a publication. However, it is worth the struggle and I don't want to see you guys give up. You can always come out with a quarterly or heck yearly [*Some people claim that we have — Ed.*].

Maybe it isn't true that you are out of the micro-race. As Mark Twain said, "Rumors of my death are greatly exaggerated." [*I couldn't have put it better — please see merger details on page 29*].

Bill Haslacher
720 S. Third St.
San Jose, CA. 95112

MERGING MAGAZINES

As has been stated in the memo on page 6, and detailed in the merger plan on page 29, MICROTREK has merged with PERSONAL COMPUTING. Benwill Publications Corporation of Brookline, Mass. has had enormous success with PERSONAL COMPUTING and has invited MICROTREK to merge with them so that our readership can enjoy a broader spectrum of small computer applications as well as a magnitude of improvement in the quality and quantity of the graphical and editorial material. I apologize for the delay in our publication schedule which was entirely due to numerous problems experienced by our small MICROTREK staff. Now that MICROTREK is appearing in the PERSONAL COMPUTING magazine, I would like to ask you send me comments regarding our new "image" and specifically how you believe it can be improved. With the new facilities at our command, I know that you will enjoy the fruits of this merger. Please note that we now have an increased need for hardware, software, and applications articles. Send outlines or complete manuscripts to: PERSONAL COMPUTING, MICROTREK EDITOR, 167 Corey Road, Brookline, Mass. 02146.



Clubs Groups and

MACH is the one

If you're in the Omaha area and wish to exchange information on construction and software development, MACH may be your speed. For meeting details of MACH (Mid-America Computer Hobbyists), contact Lt. Tom Smith at 2708 Calhoun St., Bellevue, Ne. 68005 or phone 292-6031.

computers French style

Ordinateur Libre is a French speaking computer group situated in Montreal. If the 75 member turn-out for the first meeting is any indication, Ordinateur Libre is going to be a popular group. Contact Real Menard, 2793 Dumont, Mascouche Prov. Que., Canada JON 1C0 for meeting details.

SMUG statistics

The SMUG (Sacramento Microcomputer Users Group) reports in their newsletter, *Push & Pop* that 60% of their members (or more accurately, 60% of their survey respondees) said they have some type of computer. Average memory (RAM) owned was 15K bytes. However, when polled to determine the membership interests, over 50% of the respondees checked a box labeled, "What are the little buggers, hardware, software." Hmm. For meeting details contact Richard J. Lerseth at SMUG, P.O. Box 161513, Sacramento, CA. 95816. Meeting details will also be published regularly in *ON LINE*.

Panhandlers Society

A new computer hobby club, less than 3 months old, has been formed for interested computerists in the Texas Panhandle. More than 30 members meet every Friday and meetings are open to anyone interested in computers. The Panhandle Computer Society welcomes communication with other computer groups, especially in Texas. All inquiries should be addressed to Tex Everett or Jerry Fewell at 2923 S. Spring, Amarillo, Texas 79103 or call (806) 373-8207.

Buster — the Robot

Several recent issues of the Amateur Computer Group of New Jersey's newsletter carried details for construction and programming of a motor-driven "robot." Based on a KIM-1 microprocessor system, the robot can be best described as three-wheeled triangular box which can be directed with great precision by either a joy-stick or a program stored in memory. The microprocessor senses the output of a potentiometer-comparator feedback circuit to make the necessary angular correction to the steering system and determines control voltages to be applied to the wheel motors. Who built this innovation — a 14 year old named Tod Loofbourrow (with some help from a TAB Books publication describing a similar robot using discrete logic). Write: Amateur Computer Group of New Jersey, UCTI, 1776 Raritan Road, Scotch Plains, NJ 07076 for details if this type of project interests you.

Assembling a microcomputer is one thing. Maintaining it bug-free is something else!

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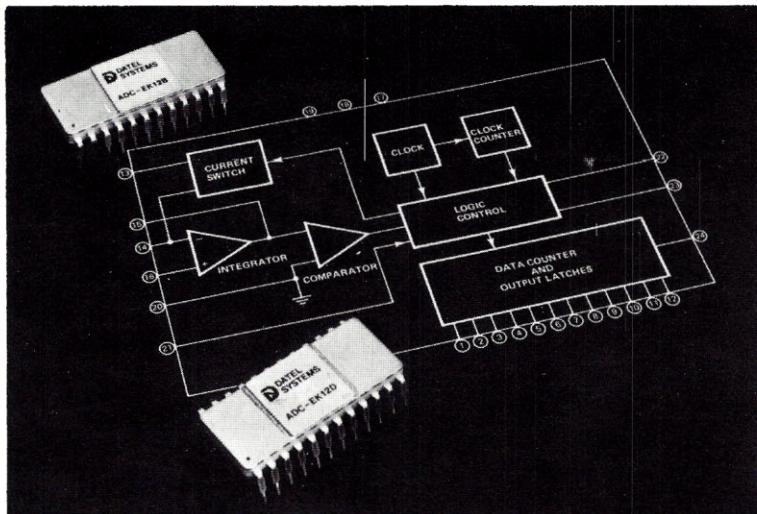
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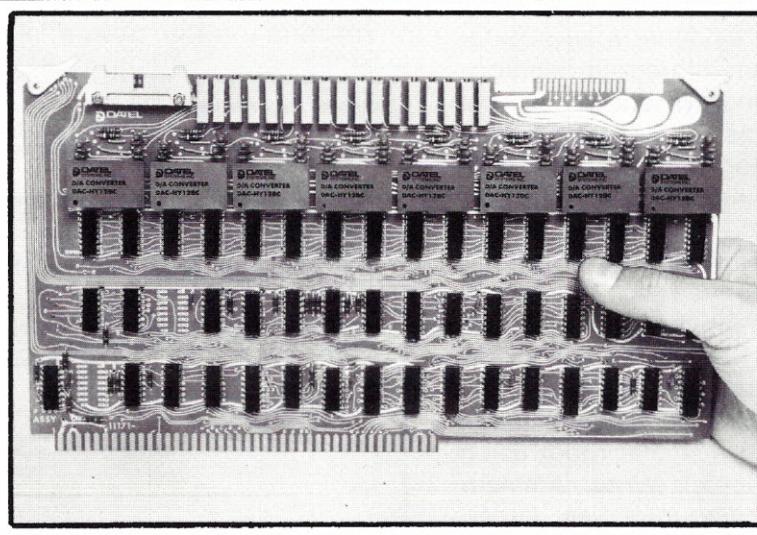
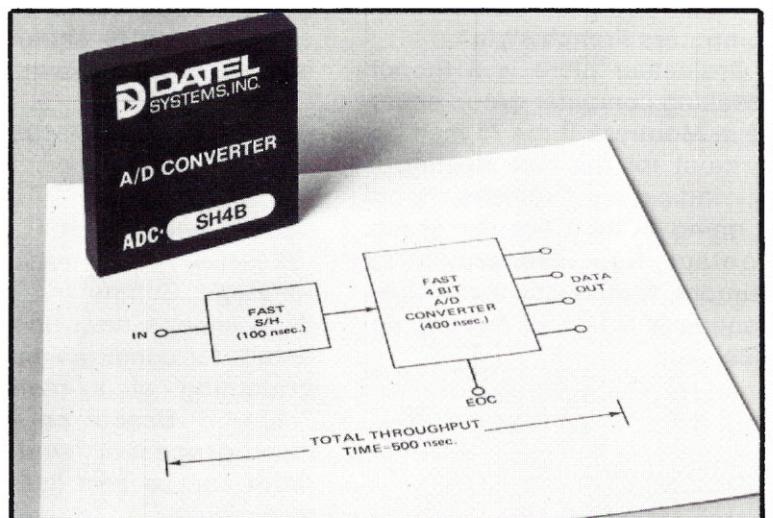


low cost CMOS A/D converter

Designed for applications requiring low power, accurate A/D conversion from slowly varying inputs, the ADC-ED series from Datel is priced from \$13.50 for a single 8-bit A/D with 0.2% relative accuracy. Conversion time is 1.8 msec. The EK converters draw 20 mW from a ± 5 VDC supply. Packaged in standard 24-pin ceramic DIP packages, the converter series consists of three binary-coded output models with 8, 10, and 12 bit resolutions. Datel Systems, Inc., 1020 Turnpike St., Canton, Mass. 02021.

ultra - fast A/D converter has built - in sample - hold

Priced at \$79 in single quantities, Datel's model ADC-SH4B 4-bit successive approximation converter contains a 100 nanosecond acquisition sample-hold circuit. A/D conversion time is 400 nanoseconds. Nonlinearity is $\pm 2\%$ maximum. The analog input range is 0 to +1 volt. Supply requirement is ± 15 VDC and +5 VDC. The unit is packaged in a 2 X 2 X 0.375 inch module. Contact Datel at 1020 Turnpike St., Canton, Mass. 02021.

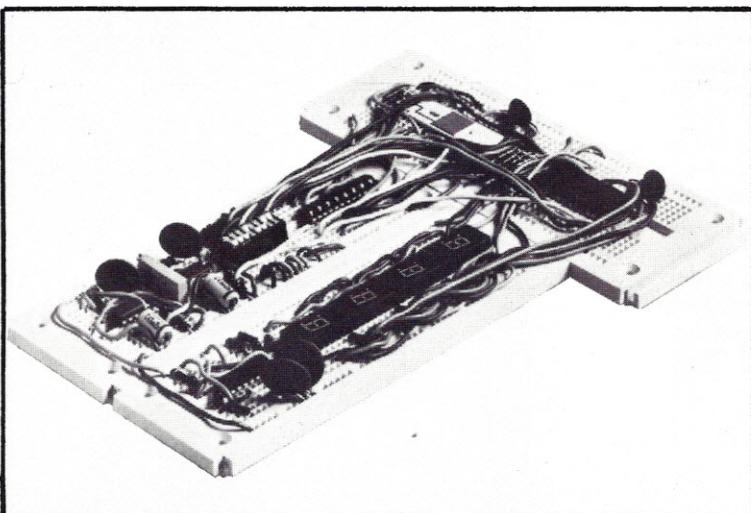
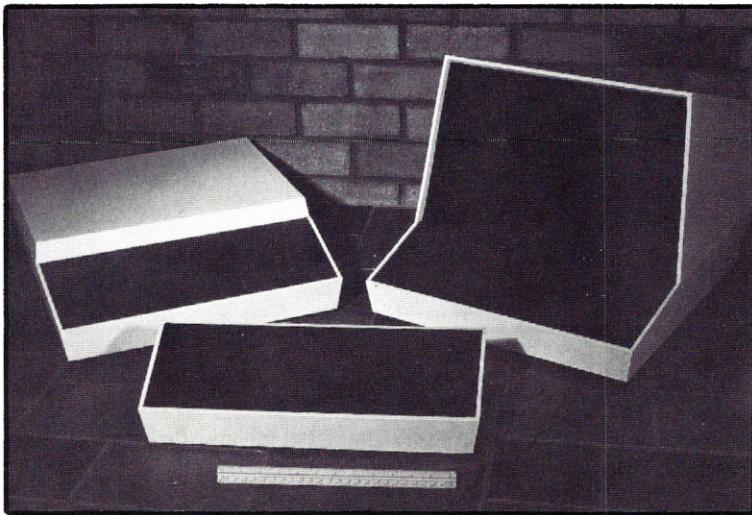


8 channel D/A card for Intel SBC-80/10 or MDS-800 bus

Industrial process control microcomputers often require one D/A output for every A/D input channel to permit computer assisted feedback control. Datel ST-800-DA8 contains 8 D/A channels on a stand-alone 12" X 6.75" X 0.375" card. Settling time of each 12-bit D/A is 4 microseconds. Two or more 2-byte instructions can be used to update each D/A channel. Included is a jumper programmable interrupt. When the last channel is reached, the processor is interrupted. Available for \$695 from Datel, 1020 Turnpike St., Canton, Mass. 02021.

inexpensive molded enclosures for CRTs and keyboards

Model VTE 101 is a CRT enclosure which measures 19 X 21 X 4 inches at the base. The CRT shroud with smoke gray plexiglass screen measures 11.25" high, 17" wide, and 12.5" deep. Model TVTE 101 consists of the same base as the CRT enclosure with a cover. Suitable for a keyboard TV typewriter. Model KBE 101 will house just the keyboard. Priced at \$77.75, \$44.45, and \$22.25 respectively. Write to: Enclosure Dynamics, Inc., P.O. Box 6276, Bridgewater, N.J. 08807.

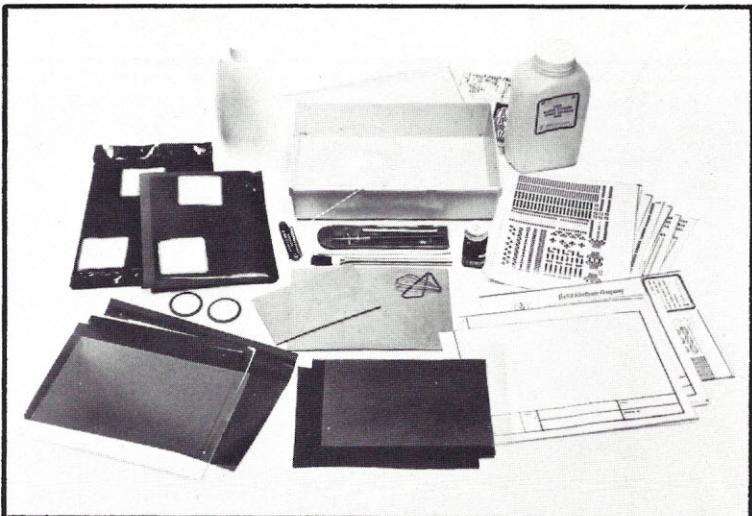


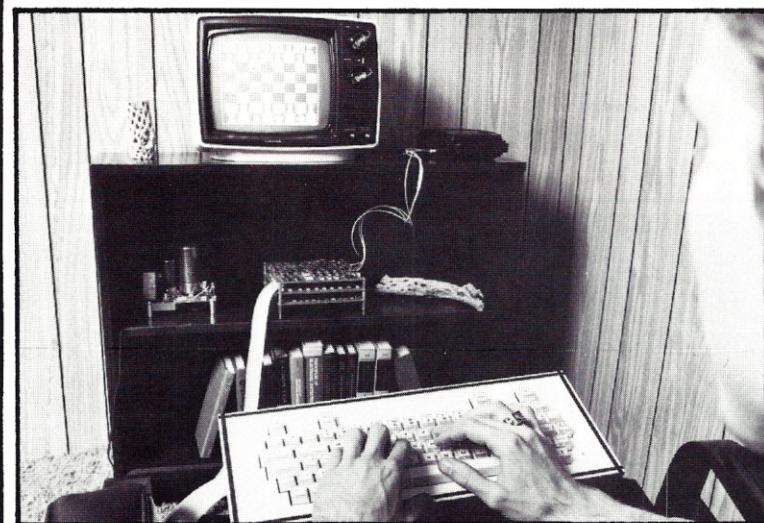
solderless breadboards for SSI/MSI and LSI DIP packages

New interlocking solderless breadboards from Continental Specialties permit optimum layout configurations for added economy. Each 6" Experimentor breadboard contains 94 5-point contacts. Experimentor model 600 has a 0.6" wide channel to seat LSI chips. Experimentor 300 seats standard DIPs and is priced at \$9.95. Contact Continental Specialties at 44 Kendall St., Box 1942, New Haven, CT. 06509 (203) 624-3103.

complete direct - etch and photo - resist PC board kits

Direct - etch boards are made by applying the acid resistant circuit patterns on the bare copper boards and etching with the ferric chloride in the kit. To make duplicate boards, layout the patterns on the mylar sheet. Expose the photosensitive boards supplied to the sun while covered with the mylar art master, and etch. Kit 32X - 1 makes two boards for \$11.50. Seven boards can be made with kit 32Xa-1 for \$28. Vector Electronics Co., 12460 Gladstone Avenue, Sylmar, Ca. 91342.





microprogrammable CPU for critical applications

Designs requiring a custom instruction set or special purpose algorithms for high speed execution are a few of the tasks which can be handled by the M - 8Z micro - programmable CPU. The M - 8Z has a micro - cycle time of 250 nanoseconds and interfaces with all modules in the System 8 line from Warner & Swasey. The module is priced at \$285, including a set of unprogrammed instruction chips for custom designs, a micro assembler (FORTRAN), and a microprogramming manual. Write: The Warner & Swasey Co., Computer Division, 7413 Washington Ave. So., Edina, Minn. 55435.



microsystem offers user defined keyboard and extensive software

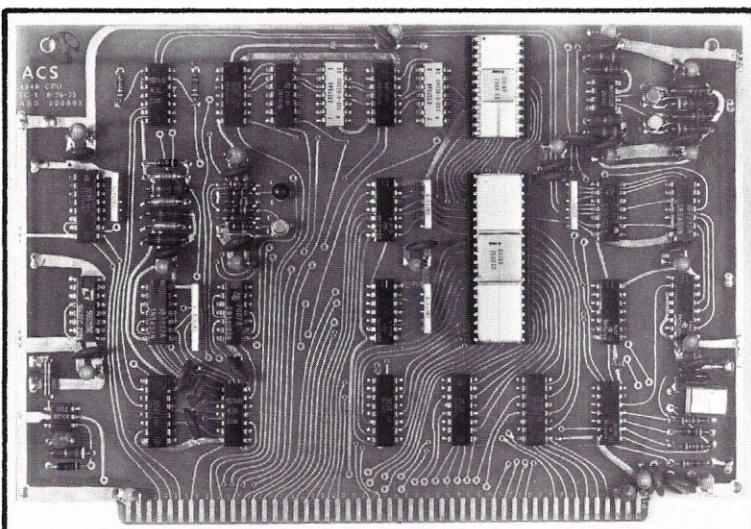
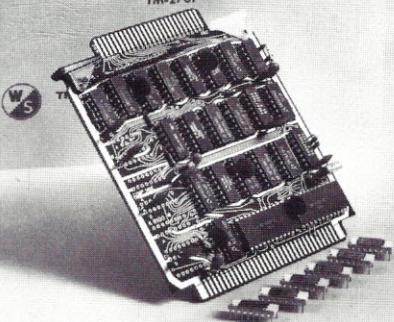


Designed for maximum operating flexibility, MICROMIND's 80 key keyboard is functionally defined with software to fit the user's application. Many types of characters can be keyed: standard 5 X 7 or 7 X 9 ASCII, APL, Japanese, Greek, Hebrew, chess pieces, etc. Custom keyboard arrangements can be configured with the relegendable keycaps supplied with the system. Software includes an interactive editor, assembler, monitor, cassette-based file system, and an extended form of BASIC language. Also, games and utilities are supplied. MICROMIND can be used as an intelligent terminal, remote job entry station, graphics display system, etc. Complete with a 6500A microcomputer, character generator, 8K of memory, input/output interface board, power supply, and 80 key keyboard, the only additional items needed are a standard television set and an inexpensive cassette recorder. Priced at \$987.54, MICROMIND is assembled and tested. Write ECD Corp., 196 Broadway, Cambridge, Mass. 02139.

Warner & Swasey System 8 Industrial Microcomputer System

MICRO-PROGRAMMING
REFERENCE MANUAL
(For M-8Z CPU)

TM-2701

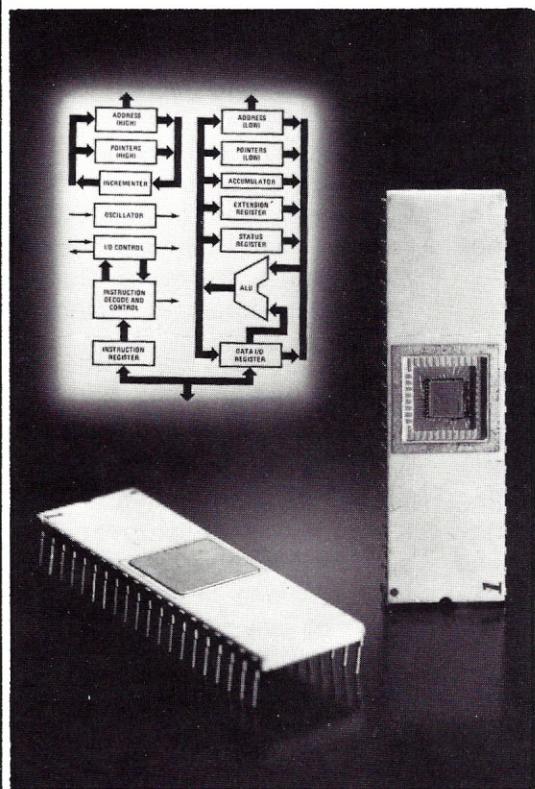


4 - bit general purpose microcomputer

The ACS - 4040 microcomputer is a parallel 4 - bit system suitable for process control, data acquisition, and front end communications controllers. Included on the ACS - 4040 board is a crystal clock, 8 bank RAM addressing, 2 bank ROM addressing, buffered expansion bus, I/O bidirectional expansion bus, Run/Single-Step mode control, Single Step input, photoisolated local/remote power and master reset. Requires +5 VDC, 0.9 Amps and -10 VDC, 0.1 Amp. Priced at \$250 (1 - 9 units): Automated Computer Systems, 2361 E. Foothill Blvd., Pasadena, Ca. 91107.

SC/MP-II: fast, low power, single voltage processor

Samples are now available of a new N-channel MOS version of the "SC/MP" 8-bit single chip microprocessor. The new SC/MP requires less than 200 milliwatts from a single +5 VDC source. Typical instruction execution time is 5 microseconds - one microsecond is required to complete one microcycle. The SC/MP-II is said to be fully compatible with its predecessor in terms of pin configuration, object code, and software. Write: National Semiconductor, 2900 Semiconductor Drive, Santa Clara, Ca. 95051.



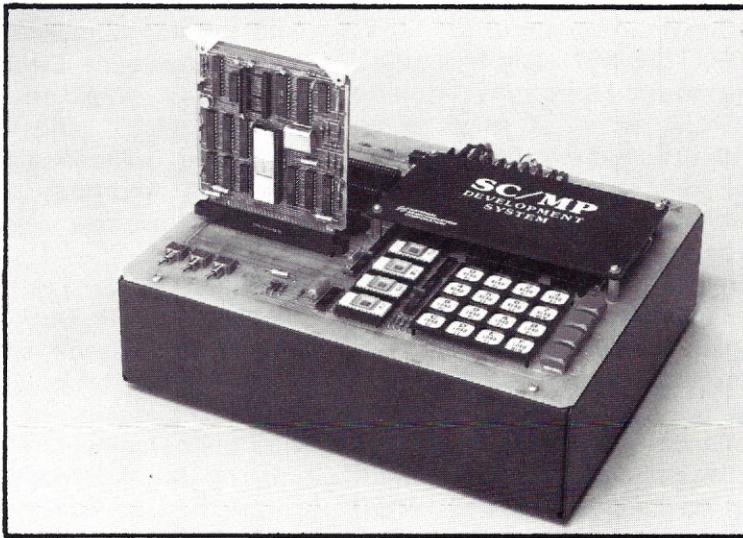
SC/MP hand - held terminal kit for \$95



The SC/MP Keyboard Kit is useful for engineers and hobbyists who wish to program the SC/MP microprocessor kit without the added expense of a teletype system. The heart of the SC/MP Keyboard Kit is a ROM firmware package of 512 bytes which replaces the "Kit Bug" ROM supplied with the SC/MP microcomputer kit. The new ROM allows the effective use of the hexadecimal keyboard, to execute programs, to examine or modify the contents of memory and the SC/MP registers, and to monitor program performance. The terminal has twenty functional keys: 16 keys for hex values 0 through F, Abort Command, Memory Command (read next memory location), Go Command, and Terminate Command (change mode of current operation). Complete with all required integrated circuits, resistors, keyboard display cable connector assembly, wire wrap connectors and wire wrap tool. National Semiconductor, 2900 Semiconductor Drive, Santa Clara, Ca. 95051.

SC/MP low - cost development system

Hardware and software designs based on the SC/MP 8-bit microprocessor can be developed and tested with the "Low-Cost Development System" (LCDS) from National Semiconductor. ROM-based firmware on the motherboard allows the user to alter the SC/MP registers and memory locations, run programs, or execute single instructions. The firmware subroutines allow entry of software debug commands via the control and display panel or an optional Teletype. \$499 from: National Semiconductor, 2900 Semiconductor Drive, Santa Clara, Ca. 95051.



New Software

MICRO BASIC PLUS

Technical Systems Consultants, Box 2574 W. Lafayette, In. 47906 has developed a highly compact version of BASIC which offers a wide range of statements, commands, and functions. Designed to run in a minimum of 4K of memory (which includes up to 60 user statements), MICRO BASIC PLUS executes much faster than most compact BASIC language packages by avoiding the slow 2-level interpretation technique commonly used to implement BASIC.

STATEMENTS

Statements available to the user include PRINT, INPUT, READ, DATA, RESTOR, IF...THEN, GOTO, GOSUB, RETURN, ON...GOTO, ON...GOSUB, FOR, with positive and negative STEP, NEXT, LET, DIM, for both single and double dimensioned arrays (up to 98 by 98), EXT, REM, and END.

COMMANDS & FUNCTIONS

Commands include LIST, SCRATCH, RUN, and MONITOR. Arithmetic functions include SIGN(X), where X may be an arithmetic expression; this function returns a value of +1 for positive arguments, -1 for negative arguments, and 0 if X is zero. The ABS function returns the absolute value of any argument. RND is a random number function: whenever RND appears in an expression it will be replaced by a random number between 0 and 99. TAB is an output formatting function: TAB(X) will move to column X, where X

can be any arithmetic expression. Function SPC(X) can be used to output a specified number of spaces.

OPERATORS

Math operators include minus, plus, multiplication, division, exponentiation, addition, and subtraction. The arithmetic range is + 99999. Relational operators include equal, less than, greater than, less than or equal to, greater than or equal to, not equal.

FEATURES

A line editor is included which permits lines to be inserted, deleted, or added at any time. Lines may be entered in any sequence; the interpreter automatically puts them in ascending order. Line lengths are limited to 72 characters. If this is exceeded, the line entered is not stored and a new "enter line" prompt is printed. Multiple statements per line are permitted using a ":" as the separator. Error identification includes 18 error codes which are printed along with the line number of the defective statement. Errors detected include syntax errors in the INPUT, READ, and IF statements, as well as many other cases of improper syntax or arithmetic overflow.

APPLICATIONS

MICRO BASIC PLUS will run on any 6800 based system which contains the Motorola MIKBUG ROM. The documentation sold with the commented source listing of MICRO BASIC PLUS shows how to adapt this compact BASIC to run on systems

which do not contain the MIKBUG routines. The commented source listing, available from Technical Systems Consultants (TSC); for \$15.95, also includes a programming example, dumping and loading procedures using paper tape or cassette, and error codes. MICRO BASIC PLUS is also available on the "Kansas City Standard" cassette for \$6.95 and paper tape for \$6.00. Write for the new Technical Systems Consultants Software Catalog (25¢ for postage and handling) for more details.

MICROCHESS

An unusual software offering is MICROCHESS, designed to play the game of chess on a KIM-1 6502 microprocessor system. The program can be adjusted to one of three different levels of play requiring 3, 10, or 100 seconds for each computer move. Although the level of play is probably below that of the serious chess player, it is a good match for the average computer programmer.

MICROCHESS program and data occupy only 1100 of the 1152 bytes of available memory on the standard KIM-1 microcomputer. All moves are entered and results displayed via the KIM-1 keyboard and hex LED display. Complete with a Player's Manual, annotated source listing, program documentation describing the strategic algorithms, instruction for modifying or expanding the system, MICROCHESS is available for \$10 from: MICROCHESS, 1612-43 Thorncliffe Pk Dr, Toronto, Ont., M4H 1J4, Canada.

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| Q1-385 | 1.5 | 9.05 | .25 | \$12.50 |
| Q1-390 | 1.5 | 9.20 | .25 | \$12.50 |
| Q1-395 | 1.5 | 9.35 | .25 | \$12.50 |
| Q1-400 | 1.5 | 9.50 | .25 | \$12.50 |
| Q1-405 | 1.5 | 9.65 | .25 | \$12.50 |
| Q1-410 | 1.5 | 9.80 | .25 | \$12.50 |
| Q1-415 | 1.5 | 9.95 | .25 | \$12.50 |
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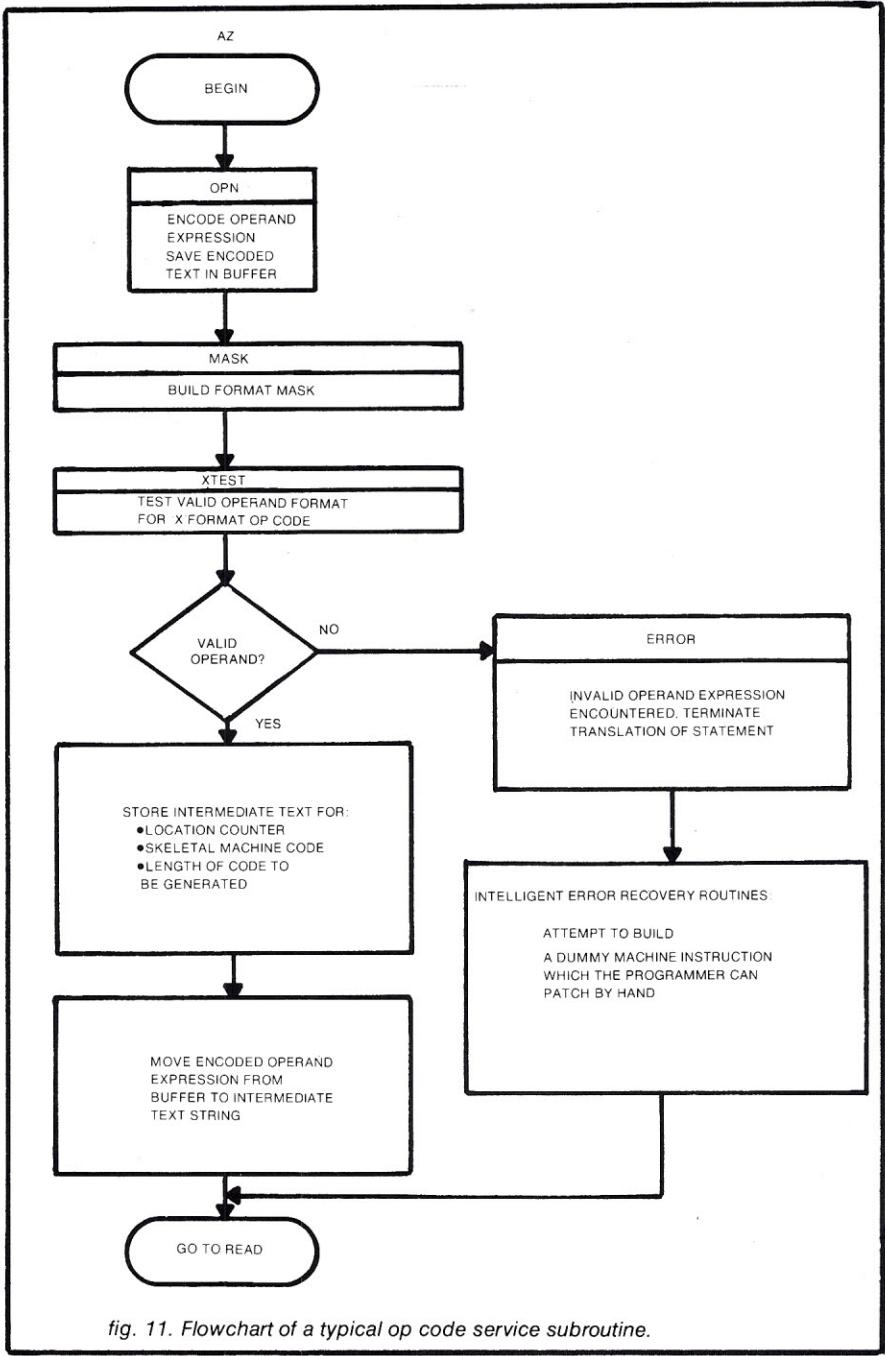


fig. 11. Flowchart of a typical op code service subroutine.

of translating this statement, the encoded operand expression, and two other important pieces of information.

One of the pieces of information is a skeletal machine instruction for the op code. Typically, each instruction for a machine has a certain amount of fixed information which is dependent solely upon the op code and a certain amount of variable information which is dependent upon the operand expression, such as addressing

modes used. One of the elements of intermediate text for a statement then is a skeletal form of the machine code to be generated with all its variable information set to zero.

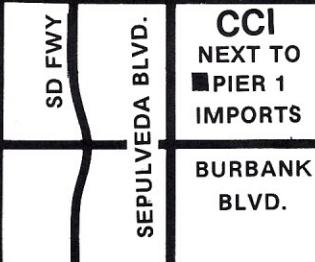
The second piece of information is an operand pattern mask. It is, in fact, used to generate the first piece of information. Typically the operands for op codes in an assembly program must all conform to a general pattern. In the sample translator the operand can, at most, be of

the format "D1(L1,X1),D2(L2,X2)". The "Dn" portions represent address or displacement expressions, the "Ln" portions are length expressions, and the "Xn" portions are index register expressions. Not all op codes can validly use this full form and most machine instructions will use only various subsets of this form, but the important thing is that all instruction operands must be in some subset of this syntactic form. The operand expression, "A+B/E,(3),X1" is of the form, "D1(X1),D2" and the expression, "Q3,5(C2,25/3)" is of the form, D1(L1),D2(L2,X2)".

There is a subroutine, MASK, which is invoked after the operand expression has been encoded. This routine examines the encoded text and returns a (bit-wise) mask indicating which elements of the possible operand format were encountered in the operand. **Fig. 10** lists the bit definitions for the mask. By examining this pattern it can be immediately determined whether or not the operand has a valid syntax for the op code and which addressing options are used. This also indicates the form and length of the skeletal machine instruction to be produced. **Fig. 11** shows how a typical op code service subroutine functions. The operand is scanned and encoded, the syntax is checked, and the intermediate text for the statement is completed.

Conclusion

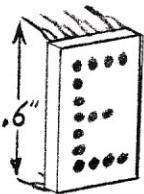
Label extraction and processing, and op code extraction and processing have been presented as a fairly simple and straightforward activity performed by a number of unique subroutines which we have examined at length. The next part of this series will deal with operand encoding which is the heart of phase one of the assembly language translator.



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